Multi-Physics Modeling of High-Power Microwave Transistors

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Abstract—In this paper, we present a multi-physics approach for the simulation of high-power microwave transistors in which electromagnetic, thermal, and nonlinear transistor models are linked together within a harmonic-balance circuit simulator. This approach is used to analyze an LDMOS transistor operating at 2.14 GHz. The total gate width of the die is 102 mm, and the die is placed in a ceramic package and connected using bond-wire arrays at gate and drain. The effects of three different gate bond-pad metallization on the transistor efficiency are studied. Plots of the spatial distribution of the drain efficiency, and time-domain current and voltage provide a unique insight and understanding of the behaviours induced by the different bond-pads.

I. INTRODUCTION

Power transistors for wireless infrastructure applications are complicated structures, comprising not only the transistor die itself, but also the in-package matching components and bond-wire arrays. These latter components, although linear, have a significant influence on the RF performance of the transistor, and must be included in a comprehensive model. These transistors are capable of delivering several hundred watts of RF power, and consequently generate and dissipate a lot of heat, so a self-consistent electro-thermal model is required. The modeling of the interconnected thermal, electromagnetic, and semiconductor device behaviours is necessary for a complete description of the transistor. Such a multi-physics modeling approach will enable the optimal design of high-power microwave transistors. Several approaches where the governing multi-physics equations are solved simultaneously have been developed [1]. While undoubtedly valuable for very small high-frequency transistors, the physical scale and consequential computational expense prohibit these approaches for infrastructure applications. Instead, the electromagnetic model, thermal model, and nonlinear electrothermal transistor models are coupled using a circuit simulator to provide a comprehensive description of the transistor in a relatively compact simulation. Several researchers have presented such multi-physics approaches, in which the effects of the matching networks, distributed parasitics, and thermal environments have been studied [2]–[4].

In this paper, we present a methodology that combines models from electromagnetic and thermal simulations with nonlinear electro-thermal transistor models in a harmonic balance simulator. We have studied the resulting effects on the

Fig. 1. A photograph of the packaged transistor along with a zoomed view of the 102-mm LDMOS transistor die. Reference planes at the package and on the die are indicated for later analysis and discussion.

device performance of using various gate bond-pad geometries. We present spatially-distributed drain efficiencies and time-domain current and voltage waveforms within the die to provide a unique visualization and understanding of the operation of these physically large RF transistors.

II. MODEL DEVELOPMENT

The multi-physics model incorporates a measurement-based nonlinear electrothermal transistor model [5], which was extracted from a 5.0-mm on-wafer transistor. The extrinsic parameters were determined [6], and the intrinsic nonlinear model was then scaled down to the unit gate width of 0.5-mm. One such model was then used to represent each gate finger in the transistor.

The thermal model is a thermal impedance matrix obtained from finite-element simulations of the transistor die [7]. Each port of this matrix connects to one of the individual gate-finger transistor models.

A combination of finite-element and moment method electromagnetic simulation software packages are used to generate a multi-port S-parameter model for the passive components surrounding the die. The finite-element method is used to simulate the package and the 3-D nature of the bonding wires. A planar simulator is then used to simulate the bonding pads. The gate and drain bond-pad structures contain approximately 100 ports, to account for the connections to the bonding wires and the connections to the individual gate and drain fingers.

Fig. 2. An illustration of the bond-pad with the port connections for the bond-wires and connections to the gates of the transistors. The metalization width, w is varied over 0, 80, 160 μm for this study.

These constituent components are generated independently, and then connected together in a circuit-theory based simulator. For efficient model assembly, we developed a systematic and automatic netlist generator, to avoid potential errors resulting from manual creation of the full transistor circuit with thousands of nodes in a schematic capture-based simulator.

We apply the multi-physics modeling methodology to study the effects on the device performance of varying the gate manifold structure. The gate manifold metallization width is adjusted from $w = 0$, 80, and 160 μm , producing a structure with almost discrete bonding pads at one extreme ($w = 160$), and a uniformly-wide structure at the other ($w = 0$). Three packaged devices were manufactured and measured in a loadpull test bench over a range of 23–37 dBm of output power at 2.14 GHz. Harmonic balance simulations were performed at the same gate and drain impedances (matched for maximum efficiency) and over the same power range as the measurements.

III. RESULTS

A. Two-Port Results

The multi-physics model using individual gate transistors should be able to produce the same two-port behaviour as is measured on the bench. The power added efficiency (PAE) is compared in Fig. 3; the model captures the measurement trends for the three cases. From Fig. 3, we noticed that the device with continuous bond-pad, $w = 0$, has approximately 20% higher efficiency than the one with discrete bond-pad, $w = 160\mu\text{m}$, in the gate manifold. To understand this, we investigated the effects of gate feed on the operation of each of the individual FETs.

B. Spatially-Distributed Effects

After a harmonic balance simulation of the transistor is complete we save all of the voltages and currents at all nodes and branches in the circuit, for all of the harmonics. Our packaged device contains 204 individual FETs, one for each

Fig. 3. A comparison of measured vs. simulated power added efficiency for three bond-pads.

gate finger, with 8 wires on the gate manifold and 12 on the drain. We save the currents and voltages at the edges of the package, the ends of the wires, and at both sides of the manifolds: this is over a thousand nodes. Simulating this circuit over a range of 15 input powers, including 3 harmonics, yields a 2 MB text file containing all of the voltages and currents.

With this information we compute the performance of each individual transistor (gate) and plot it as a function of its position along the manifold. In Fig. 4(a) we plot the drain efficiency vs. input power and the location of each pair of transistors connected to the drain bond-pad. For the wide gate bond-pad, $w = 0$, the efficiency shows double peaks, with lower efficiency at the center of the die. For the discrete bond-pad, $w = 160\mu\text{m}$, the drain efficiency surface is remarkably different, with the center of the die having a negative efficiency, as shown in Fig. 4(b). Although not shown here, due to space limitations, we have verified through measurement and simulation the thermal behaviour of the transistors, and shown that it does not have a substantial influence on these results, due to the wide spacing between the gate fingers.

We have also examined the time-domain waveforms for each individual FET in the whole device. Using the harmonic voltages and currents from the harmonic balance simulation we constructed the time-domain waveforms for each individual transistor within the die. In Figs. 4(c) and 4(d) the voltages applied to the each gate, the resulting drain current, and the drain voltages are plotted vs. position and time. For the discrete manifolds, the transistors in the center of the large die are turning on at a later time than the transistors at the edges of the device. This is because there is a voltage distribution caused by the bond-pad and wires connecting to the transistor, as noted by Goverdhanam [3]. The transistors at the center of the die are delayed in their gate voltage excitation, so the drain current and drain voltage are now in phase (overlapping), resulting in a large power dissipation in this part of the structure, as shown in Fig. 4(d). This gives the 20% efficiency loss shown in Fig. 3.

(a) Drain efficiency for the gate manifold with $w = 0\mu\text{m}$. (b) Drain efficiency for the gate manifold with $w = 160\mu\text{m}$.

(c) Time-domain waveforms for $w = 0\mu\text{m}$.

(d) Time-domain waveforms for $w = 160\mu\text{m}$.

Fig. 4. The effects of two different bond-pad gate metal layouts, $w = 0$ and $w = 160\mu\text{m}$, are plotted. In (a) and (b) the drain efficiency is plotted for each individual transistor model as a function of input power. The time-domain waveforms at the gates and drains are shown in (c) and (d). Note that although this FET contains 102-mm of total gate periphery, several drains have not been connected in the final layout, these are showing in (a) and (b) as missing data, and in (c) and (d) as vertical lines that are not contributing to the overall performance. In (c) and (d), the index, refers to either the number of connections to the gate or drain bondpads from the transistor assembly.

IV. CONCLUSION

The multi-physics based modeling methodology enables greater understanding of the operation of microwave power transistors. By plotting the drain efficiency and time-domain waveforms for all individual transistors in the die we get unique insight into the behaviour of the power transistor. The gate bond-pads were shown to have a large influence on the transistor performance, where, in the worst case, transistors at the center of the die were dissipating rather than generating power. It is very unlikely that the cause of this poor performance could have been deduced from the measured 2-port parameters of the transistor.

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