Advanced Technologies for Next-Generation RF Front-End Modules

(Invited Paper)

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Abstract – The complexity of RF front-end (RFFE) modules of wireless devices has increased dramatically over the past decade. In order to meet the demands for future mobile communications, RFFEs will need to enable multiband for global roaming, and multi-mode to support multiple cellular modes, incorporate beamforming antennas, and operate at mm-wave frequencies. To this end, this paper presents a summary of the recent progress in RF substrate technologies, waveguide architectures and multi-band design techniques for 5G RFFE modules, and summarizes the present and future challenges in RFFE module design.

Keywords– Millimeter-waves, RF front-end modules, gap waveguides, substrate integrated waveguides (SIW).

1. Introduction

The telecommunication revolution of the early 21st century has led to a proliferation of wireless devices, and recent estimates have shown that there is almost one handset for every person on earth. In a cellular handset, the RF front-end (RFFE) and antenna combination establishes the quality of the wireless link between a handset and the base-station. The front-end module can be viewed as a group of RF devices that enable high frequency transmission and reception of voice, data and control signals between the handset and network [1]. Functionally, an RFFE provides the majority of the analog signal processing including signal filtering, detection, amplification and demodulation. Figure 1 illustrates a schematic of a RFFE module with its constituent sub-circuits including power amplifiers, switches, filters, duplexers and low noise amplifiers (LNAs). To meet the demands of successive mobile generations, RFFE modules require an ever-increasing integration, squeezing more functionality into a single chip [2]. Consumer electronics have concomitant demand for data and increased usage of electromagnetic spectrum. From four bands in early 2000s to support 2G, mobile communication systems now use more than 30 bands and this will continue to increase for 5G (Figure 2). For 5G cellular systems, the frequency ranges are 24.5 to 29.5 GHz and 37.0 to 43.5 GHz for 28 and 39 GHz spectrum, respectively. A new Wi-Fi standard IEEE 802.11ad that operates in the 60 GHz band (V-band 57-64 GHz) to achieve as much as 7 Gbps data transfer rate is also under development. As mobile phone data requirements continue to grow, the complexity of the RFFE and requirements for higher-frequency operation creates new challenges for design.

Figure 1. A schematic for a state-of-the-art RF front-end module showing the power amplifier and receiver diversity modules [2].

A highly-integrated 5G system architecture consists of several components such as 1) integrated circuits, e.g. PA, mixer, LNAs 2) transmission lines 3) passives 4) antennas 5) interconnects and 6) substrates (core and buildup). Requirements for each successive mobile communication generation are higher linearity and isolation, lower costs, lower power consumption, multi-band/multi-mode capability, and smaller product size [1]. In addition, to design inexpensive devices for the internet of things (IoT), RFFE will need to be designed with a minimum number of components, and manufacturing volumes will have to increase dramatically to reduce per-unit costs. Advances in substrates, multi-band passive devices, and packaging, such as system in package (SIP) technologies, are also required to continue to drive maximum integration.

Figure 2. The rising number of supported bands versus time (partial data obtained from [3]). As a result, this necessitates an increase in the RFFE complexity.

There have been numerous advancements in substrate technologies for wireless applications and devices. Among them, CMOS substrates such as bulk Si, high-resistivity (HR)-silicon on insulator (SOI), surface acoustic wave (SAW) substrates including LiNbO_3 and LiTaO_3 , and flexible substrates such as Kapton and PET have been widely explored by the research community to circumvent some of the traditional design limitations including such as cross talk, power dissipation, environmental friendliness, and lower per-unit cost.

Millimeter (mm)-wave wireless connectivity is considered to be one of the major strengths for 5G networks as it can support significantly a larger bandwidth and allow narrower beam widths

and miniaturized hardware. Wireless devices operating in mm-wave frequency range have limited applications due to high path loss and attenuation. Additionally, due to small device dimension and fabrication tolerances, it is challenging and expensive to fabricate high-performance mm-wave components like antennas and passive devices, by using conventional technologies like microstrip or coplanar waveguides. Hence, there is a definite need for novel waveguide topologies that offer higher-Q factors, and lower loss at frequencies at 30 GHz and beyond. Furthermore, as RF packaging is essential for high-density microwave modules operating at mm-wave frequencies, such waveguide topologies must be compatible with packaging solutions. To this end, two innovative integrated waveguides, i.e., gap waveguide and substrate integrated waveguide (SIW) have been proposed [3].

Figure 3. The RFFE innovation triangle showing the materials, architecture and design relationship [3].

For 5G, the power consumption and size of constituent components in an RFFE have an important role in the overall behavior of the wireless systems. Techniques of designing components that exhibit multi-band operation have the potential to achieve compact size and low power consumption. “Innovations that enable 5G RFFEs will need to include a low-loss triplexer, multi-mode, multi-band PAs, and multi-band filters, all of which need to be optimized as a complete system to reduce matching components” [4]. If multiband components can reduce the number of antennas, filters, and switches, this will minimize the module volume and cost of production for 5G equipment.

Motivated by these challenges, the requirements for an advanced RFFE module can be summarized in the RFFE innovation triangle illustrated in Figure 3. And in this paper, we summarize the latest research and concepts for each area listed in Figure 3. As the substrate is the first consideration for an RFFE design, we first discuss the conventional substrate technologies capable of addressing the design requirements. Further, novel materials and their characterization methodologies have been discussed to demonstrate their applicability for future RFFEs. Subsequently, two state-of-the-art waveguide topologies for mm-wave RF component design, namely, gap waveguide and SIWs are discussed. Emphasis is focused on gap waveguide-based antennas and SIW-based diplexers as antennas and diplexers are crucial components in RFFE transceivers. Finally, novel design techniques for dual band passive component design are exemplified using a Wilkinson power divider (WPD).

2. Recent Progress in Substrate Technologies

RF substrates have a major role in the growth of the RFFE market and this market is worth US\$6 billion. In a packaged RFFE module, the substrate acts as a carrier to support the die, provides the interconnection and distribution of signals and ground to various components and other die, and finally allows passive devices to be embedded. This section provides an overview of state-of-the-art developments in substrate technologies that will enable mobile devices for the next decade.

A. Semiconductor Substrate Technology:

Materials such as gallium arsenide (GaAs), alumina, and silicon on sapphire (SOS) have been the traditional substrate of choice for microwave and RF applications. Over the years, heavily-doped or low-resistivity silicon wafers were used as substrates for CMOS. These wafers have substrate resistivities in the range of $0.05 \Omega\cdot\text{cm}$. However, with recent advances in system-on-chip (SOC) designs, increases in the substrate resistivity were made to improve the noise isolation and reduce the coupling between devices. High-resistivity silicon wafers with resistivity in the excess of $1000 \Omega\cdot\text{cm}$ were introduced to improve the isolation. Table 1 shows the recent technologies of choice for each component in a RFFE module [5].

GaAs has a high mobility, a high breakdown voltage, low loss and high linearity, all of which are essential for LNAs [4]. However, for SOC configurations, GaAs faces some limitations

TABLE 1 Technologies of choice for RFFE [5]		
	Key Substrate Parameter	Recent Market Technology of Choice
Switch	Linearity Resistivity	GaAs pHEMT, SoS, HR-SOI
Power Amplifier	Carrier mobility Thermal dissipation Linearity Resistivity	GaAs HBT, LDMOS
Power Mgt Unit	Thermal dissipation	HV CMOS
Filter	Resistivity Piezoelectricity	SAW, BAW, IPD, SMD

in terms of digital integration. High Electron Mobility Transistors (HEMTs) have been historically used for high-speed applications because of their relatively higher current gain cut-off frequency and maximum oscillation frequency. To alleviate integration issues, new GaAs processes such as BiFET or Bi-HEMT are now being developed to enable grouping of different functions, such as linear power amplification, logic and control circuitry, RF switching, and low noise power amplification on a single die for RFFE module integration.

In contrast, bulk Si provides a compromise for integrating high-quality digital circuit and standard RF capabilities. The major issue with bulk Si substrates for RF are poor linearity and significant attenuation. To improve system integration using bulk Si, various process options are required such as triple wells and deep isolation trenches [7]. Therefore, in the early 2000s, silicon-on-insulator (SOI) was introduced as a remedy for dielectric insulation in MOS devices. SOI electrically insulates the thin layer at the wafer surface carrying the electronic devices from the bulk wafer used as mechanical support [5]. SOI offers several advantages including reduced source and drain capacitances, higher transconductance, and dielectric isolation. Silicon-on-sapphire (SOS) is one type of SOI wafer and in fact, the first SOI wafer fabricated. SOS substrates are well suited for RF/microwave devices as they provide good isolation between devices and can easily integrate both high-speed digital and RF circuits on the same chip. This material has all the performance attributes required for RFFE module integration, and to combine power amplifiers, switches, and antenna tuning on a single chip. There are two types of SOS substrates available: epi

SOS and bonded SOS. Among the two, the latter is built using transfer processes and direct wafer-bonding to transfer and bond a high-quality thin silicon layer onto a sapphire substrate. The resulting bonded SOS substrate offers high transistor mobility and Si quality thus making it ideal for enhanced RFIC performance, functionality, and form factor, enabling IC size reduction while increasing performance by as much as 30 percent [6]. Nevertheless, in the context of low-cost integration, high-resistivity silicon wafers are needed to improve the performance of passive components, and substrate electrical isolation between the integrated digital, RF and analog components. HR-SOI satisfies almost all the conditions needed for the integration of high speed digital and RF circuits on the same chip. It has low RF noise, good linearity, and high breakdown voltage; better thermal conductivity than SOS and GaAs; and high programmability as bulk Si, making it the most suitable for SOC. Owing to its advantages for RF and SOC, HR-SOI has attracted interest from several research groups [8-11]. Figure 4 depicts the comparison of different performance attributes of GaAs, SOS, HR-SOI and bulk Si substrates.

Figure 4. CMOS substrate and process performance versus ideal target [5].

From Figure 4 it is clear that HR-SOI has advantages for 5G RFFE, however, research efforts on the substrate characterization are required for two reasons :1) drive further improvements on fabrication process 2) monitor fabricated substrates and their quality during mass production.

Several researchers have reported on the electrical characteristics of bulk silicon and HR-SOI. In [6], a capacitance-voltage (C-V) method based characterization technique was adopted to measure the electrical properties of HR-SOI substrate. In addition, it was shown that as the substrate resistivity increases, the coupling between the devices also increases, which lowers the coupling through the substrate. A significant reduction on crosstalk was observed in the frequency range of 1-10 GHz when the substrate resistivity was increased from $10 \Omega\cdot\text{cm}$ to $1.2\text{k} \Omega\cdot\text{cm}$. However, it is noteworthy that, HR-SOI substrate suffers from resistivity degradation due to the formation of parasitic surface conduction (PSC) beneath the buried oxide layer due to fixed oxide charges (Q_{ox}) within the oxide. The buried oxide layer is referred as BOX. One of the most efficient techniques to overcome this problem is to introduce a trap-rich layer at the Si/SiO₂ interface compatible with industrial SOI wafer production and thermal budget of standard CMOS process. Such a layer aims to capture the free carriers forming the PSC and thus retaining the substrate nominal high resistivity. In [12], the authors presented two types of trap-rich HR-SOI wafers to enhance the signal integrity. eSI HR-SOI substrate with a BOX thickness of 400 nm and 200 nm, respectively, were developed by SoitecTM (Figure 5). These substrates were then studied and compared with the classical HR-SOI substrate with a BOX thickness of 1 μm . Key attributes such as non-linearity effects, crosstalk, noise coupling, DC/RF figures of merit and self-heating were considered for the comparison.

Figure 5. eSI HR-SOI substrate with tap-rich layer to address parasitic surface conduction in traditional HR-SOI. The tap-rich layer freezes the highly conductive layer at box [12].

The test structures in [12] included 0.52 μm -thick CPW lines and PD SOI nMOSFETs fabricated using TowerJazz's 0.18 μm SOI CMOS process. To investigate substrate coupling, the authors used a passive crosstalk structure consisting of two identical metallic RF pads for probe

measurement. Further, the effective resistivity (ρ_{eff}) and loss (α) on the three different types of substrates were extracted from S-parameter measurement of a 2100 μm -long CPW line. Figure 6 shows that due to the formation of PSC, the conventional HR-SOI substrate loses its nominal high-resistivity and shows an effective resistivity of only 200 $\Omega\cdot\text{cm}$, whereas in 1st and 2nd generations of trap-rich eSI HR-SOI, the resistivity is more than 2 $\text{k}\Omega\cdot\text{cm}$ and 3 $\text{k}\Omega\cdot\text{cm}$, respectively, up to 5 GHz. Furthermore, it can be seen that the eSI Gen2 HR-SOI substrate shows a slightly higher ρ_{eff} and lower α compared with eSI Gen1 HR-SOI. This can be attributed to the higher nominal substrate resistivity in 2nd generation.

Figure 6. (a) Effective resistivity (b) Total Loss of 3 different substrates of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich HR-SOI (eSI Gen2) and conventional high resistivity HR-SOI [12].

To address the stringent requirements of multi-mode cellular phones and 5G standards, it is imperative to investigate the non-linear behavior of possible sources of non-linearities, in particular, the harmonic distortion from lossy Si substrates on which the RFFE is integrated. Figure 7(a) shows the 2nd harmonic distortion at the output of CPW lines for HR-SOI, eSI Gen1 and eSI Gen2 wafers as reported in [12]. Here, the output of the CPW lines on different wafers were fed by 900 MHz input RF signal with zero bias and power level ramp of -25 dBm to 25 dBm. As can be seen, compared with HR-SOI wafer, a reduction of 24 dB was measured on both generations of trap-rich eSI HR-SOI for the 2nd harmonic. A similar trend can be observed for the 3rd harmonics as well, where a reduction of 35 dB was observed. Figure 7(b) reports the cross talk analysis of different wafers for the test structures that appears as inset. Capacitive coupling was

observed for both eSI Gen1 and Gen2 with a typical 20 dB/decade slope over the entire frequency range of 150 MHz-to-3 GHz showing the lossless nature of the eSI HR-SOI substrates. Also a reduction of 15 dB of crosstalk was observed at 200 MHz for trap-rich HR-SOI wafers compared with its conventional HR-SOI counterpart. From Figure 7(b) it can be seen that HR-SOI substrate suffers from a higher crosstalk level (slope >20 dB/dec) due to the PSC effect which is suppressed in eSI HR-SOI wafers [12].

Porous Si (PSi) is another popular material that can be formed on an Si wafer and provides an adequate platform for the integration of high-performance RF passives [13]. PSi exhibits adjustable properties, which can be adjusted to meet the RF requirements such as low dielectric permittivity, high resistivity, CMOS compatibility and local information on Si wafer in a CMOS-compatible way. The low relative permittivity of PSi compared with bulk Si ($\epsilon_{r, Si} = 11.9$) is one of the main properties that makes it very appropriate for use as a low-loss, RF substrate for the monolithic integration of RF and mm-wave passive devices with CMOS.

Figure 7. (a) 2nd harmonic distortion measured at zero bias by CPW lines on 3 different wafers (b) Measured crosstalk vs frequency on HR-SOI, eSI Gen1 and eSI Gen2 HRSOI substrates [12].

Many attempts have been made to extract the dielectric permittivity of PSi using C-V and broadband measurements. Figure 8 depicts the permittivity and loss tangent of PSi extracted from broadband measurements. It can be observed that the permittivity of the high-porosity material (70 %) is less than 4, whereas the value of loss tangent is found to be between 0.01 and 0.04.

Figure 8. (a) Dielectric permittivity (b) Loss tangent in the frequency range of 1-40 GHz and 140-210 GHz of PSi extracted from broadband electrical measurements [13].

It is noteworthy that while Si based substrate technologies are better suited for mobile handsets due to cost, battery voltage and RF power requirements, GaN is still a natural candidate for base-station deployment. Since today's base station PAs require high output power, they are largely designed in GaN at higher frequencies [13]. For example, GaN devices are capable of operating at a RF power density of 6-8 W/mm of gate periphery at 4G cellular bands and can deliver an impressive power density of 3.6 W/mm at 86 GHz in continuous mode operation. Furthermore, an output power of 3.6 Watt at 83 GHz has also been reported in pulse operation. However, Si based technologies offer several advantages resulting in higher monolithic integration with added functionalities (e.g. on-chip digital control, adaptive matching, and digital pre-distortion), that translates to lower costs and smaller sizes for broadband multimode multiband 5G RFFE [14]. Nevertheless, there has been continual efforts from industry and academic researchers to customize GaN for lower operating voltages and higher operating frequencies, thus enabling the design of switches, LNAs and frequency conversion circuitry. Recent advances in GaN technology for 5G PA design is beyond the scope of this article and will not be discussed here. Interested readers can refer to [13], [14] for in-depth discussions on future research trends of GaN technologies for 5G PA design.

Through intensive collaboration between academia, wafer foundries, and mobile RFFE component manufacturers, HR-SOI has today largely displaced traditional III-V and SOS substrates due to its improved performance, reduced size and excellent manufacturing yields, and low costs. Another major advantage, when compared with III-V and sapphire-based technologies,

is that HR-SOI technologies typically employ the exact same back-end-offline metallization, bumping, thinning and copper pillar, and other post-processing technologies utilized in conventional silicon bulk technologies with no needed modification or added costs [2]. RF-SOI solutions are now present in essentially every major handset platform, providing performance in increasingly complex multi-throw RF switches, tunable RF capacitance arrays, and antenna RF tuners. On the other hand, RF filters impose stringent technical challenges such as high quality factor, low insertion loss, high out of band rejection, frequency tolerance $>1\%$ and smaller physical dimensions that has motivated the research into alternative substrate technologies. It is noteworthy that, the state-of-the-art smartphones accommodate more than 60 filters and command the largest share of the RF wallet.

B. Acoustic Wave Substrates:

Acoustic wave substrates are widely adopted to design RF filters and sensors. In addition to their small size, acoustic wave devices offer high-quality factors that result in low insertion losses (a smaller insertion loss leads to a longer battery life and a better signal-to-noise ratio) as well as steep filter flanks; steeper filter flanks allow more efficient use of the frequency spectrum [16]. A recent report from *Yole Development* predicts the RF filters will grow in to a US \$17 billion market by 2022 [3]. An in-depth discussion of different topologies for RF surface acoustic wave (SAW) filter design has been already provided in literature [17, 18]. However, it should be noted that, before the design and implementation of any component in an RFFE, the dielectric constant and loss tangent values of the substrate must be precisely known. This enables the engineers to design interconnections with correct characteristic impedances and known propagation delays [2]. Normally, during the design process, the values provided in the datasheets which are average values dependent on the fabrication process are utilized. However, when the complexity of the circuit requires high accuracy, substrate characterization is paramount. This is especially true for new flexible substrates and printed technologies. Therefore, we will focus on the state-of-the-art characterization for SAW substrates in this section. Substrates with low propagation loss per wavelength is a prerequisite for RF filters exhibiting low insertion attenuation. In addition, substrates exhibiting low temperature coefficient of frequency (TCF) are desired. Generally, such substrates are created by applying a thin layer of SiO_2 or by wafer-bonding techniques.

To study the effect of SiO₂ on attenuation properties, several sets of CPW lines was fabricated on LiNbO₃ substrates with and without the oxide coating in [19]. The microwave characterization of the CPW lines was performed through on-wafer measurements up to 40 GHz. The complex propagation constant, $\gamma = \alpha + j\beta$, for the CPW lines were extracted following a Thru-Reflect-Line (TRL) calibration approach [19]. In this approach, the complex propagation constant is extracted by solving an eigenvalue problem of measured raw S-parameter matrices for pairs of transmission lines with different lengths. Furthermore, eight test structures were manufactured in this study with different dimensions, where samples a-d were fabricated without oxide layer and samples e-h were fabricated with 0.46 μm thick oxide layer. It can be seen from Figure 9(a) where the square of the attenuation, plotted against frequency for the samples a-d exhibit a linear behavior. In contrast, lines e-h with oxide buffers typically show a superlinear behavior of the square of the attenuation as shown in Figure 9(b). Here, the linear term in the frequency-dependence of the attenuation can be attributed to dielectric losses in the SiO₂ layer. It was further noticed that, the excess losses in the lines with oxide buffer compromises the frequency performance of the electrodes and hides the advantages obtained at high frequency by reduced refractive index [19].

Figure 9. Behavior of square of attenuation with frequency for LiNbO₃: (a) no oxide buffer (b) with oxide buffer [19].

Similarly, in [20], the authors reported a dielectric characterization of LiNbO₃ using CPW lines. In this case, LiNbO₃ crystal was used as the substrate without an oxide coating. The propagation constant γ of the CPW lines was derived from the transmission or *ABCD* matrix (obtained from two port S-parameters). The effective dielectric constant ϵ_{eff} was then extracted

from the phase constant (imaginary part of γ). Finally, the relative dielectric constant of the LiNbO₃ crystal and the characteristic impedance as a function of frequency were extracted from the effective dielectric constant using conformal mapping [20]. From Figure 10(a) it can be observed that the extracted dielectric constant of the LiNbO₃ crystal is 30 ± 1 and the characteristic impedance of the CPW lines is 22Ω . Furthermore, as can be seen in Figure 10(b), the conductor loss dominated in the lower frequency band and below 10 GHz, the reported structure had a dielectric loss of 0.1 dB/mm greater than conductor loss. The dielectric loss was further utilized to obtain the loss tangent for LiNbO₃ which was found to be 3×10^{-3} at 2 GHz, 3×10^{-3} at 4 GHz, 5×10^{-3} at 8 GHz, and 7×10^{-3} at 16 GHz. It is noteworthy that, these values are not negligible even for X-band applications. Nevertheless, for LiNbO₃ as a microwave substrate, the dielectric quality factor is between 100 and 1000, which makes it appropriate to use at RF/microwave frequencies.

Figure 10. Extracted (a) Characteristic impedance and dielectric constant (b) Attenuation as a function of frequency for LiNbO₃ crystal [20].

Lithium tantalate (LiTaO₃) is another widely used piezoelectric material because it has a high curie temperature of 610°C, large saturation polarization of 60 $\mu\text{C}/\text{cm}^2$, and small dielectric constant. In [21], authors reported the thermal, optical and dielectric characterization of LiTaO₃ films deposited on Pt/Ti/SiO₂/Si substrate by the sol-gel method. Figure 11 depicts the frequency dependent dielectric constant and loss tangent of multilayer LiTaO₃ films annealed at 650°C. The dielectric constant and loss tangent of LiTaO₃ are reported to be 43-47 and lower than 0.01 in previous studies [16, 22]. However, [21] shows that in case of thin films, the dielectric constant and loss tangent are strongly influenced by the growth conditions, orientation, nature of electrodes used and interfaces between these films. Here, the dielectric constant decreases rapidly and the loss tangent rises slightly with an increase in frequency. The value of the dielectric constant for

multilayer LiTaO₃ films at 10 kHz was found to be 19.8 which is less compared to that of single crystal (Figure 11). The loss tangent was around 0.06.

Figure 11. Dielectric permittivity and loss tangent as a function of frequency for LiTaO₃ thin films [21].

Research is now focusing on robust, efficient, and cost-effective methods of fabrication for the mass-production and to reduce the cost of RFFE for cellphones. To this end, printed electronics on flexible substrates has evolved as a promising solution for low cost mass production of RFID based sensors and microwave components. However, to fully understand the applicability of printed electronics for next generation RFFE, it is imperative to study the frequency-dependent behavior of its constituent materials.

C. Flexible Substrate Technology:

Over the past decade, the interest in both academia and industry for flexible electronics has risen enormously as flexible substrates can be conformably shaped, are elastic, lightweight, and non-breakable. Furthermore, flexible substrates are also of significant interest for wearable technologies, for on-body communication and to develop inexpensive and portable medical devices. Additionally, the IoT which is expected to revolutionize and connect the world via heterogeneous smart devices through seamless connectivity. Driven by the perpetual demand for sensors acting as data sourcing platforms or emerging smart devices, the global RFID sensor market has grown to US \$20 billion in 2018. Amid the increasing difficulty of manufacturing these RFID sensors at low-per-unit cost, the need for an inexpensive manufacture of environmentally

friendly electronics has become paramount. Recently, printed electronics has emerged as an alternative to conventional manufacturing techniques such as etching and milling as it enables realization of low-cost, large area, high-throughput, lightweight and disposable electronic devices on flexible substrates using fast printing techniques at room temperatures. Recent market analysis show with the evolution of 5G and the IoT, the total market of flexible electronics will grow from US \$26 billion in 2016 to US \$69 billion in 2026 [3, 4, 24].

Materials used for flexible substrates are broadly categorized into two sections: organic and inorganic. Organic substrate materials such as, polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyimide (PI), liquid crystal polymers (LCPs), and paper-based substrate are widely used for RF/microwave applications. Whereas thin glass and metal foil remain as popular choices for inorganic substrate materials. Table 3 provides a comparison of material properties of different organic substrates [24].

TABLE 2 Properties of organic flexible substrates [22]					
Material	PET	PEN	Kapton	LCP	Paper
Dielectric Constant	3.3~3.4	~2.9	3.2~3.4	~3.1	~3.2
Loss Tangent	~0.01	~0.025	~0.002	0.002~0.005	~0.007
Melting Point	~260 °C	~265 °C	NA	285 °C~315 °C	NA
Glass-Transition Temperature	78 °C	121°C	410°C	NA	NA
Chemical Resistance	Good	Good	Good	Excellent	NA
Mechanical Properties	Good	Good	Excellent	Good	NA

In conventional processing, photolithography, chemical etching, and physical vapor deposition coating processes are combined to fabricate metallic patterns, on a flexible substrate. Recently, direct printing technologies have emerged as an alternative that can significantly simplify fabrication and dramatically reduce the manufacturing costs. Thus, many traditional printing methods such as gravure printing, flexography, screen printing, and inkjet printing are making inroads into electronics manufacturing. Significant effort from the scientific community

has been devoted to extract the material properties from measurements of inkjet and screen printed components at RF/microwave frequencies. Some studies proposed extraction of propagation constant and characteristic impedance using S-parameter measurements [25, 26]. In [25], the authors extracted the characteristic impedance and propagation constant from $ABCD$ parameters of inkjet printed CPWs on quartz. The $ABCD$ parameters were derived from the measured S-parameter matrix using well-known formulas [25]. Figure 12(a) depicts the extracted propagation constant and characteristic impedance for inkjet printed CPW lines on quartz. Whereas Figure 12(b) shows the effect of copper electroplating on insertion loss for inkjet printed CPWs on Kapton. It was observed that the insertion loss drops from -12 dB to approximately -1.5 dB with copper electroplating. A single probe measurement using two inkjet printed concentric circular capacitors with different gap sizes were utilized to characterize the complex dielectric properties of flexible substrates in [27].

Figure 12. (a) Extracted propagation constant and characteristic impedance from [25] (b) Measured insertion loss for inkjet printed CPWs with and without copper electroplating [26].

In [27], the dielectric constant and loss tangent of Kapton, LCP, and PET were measured from 50 MHz to 20 GHz. The plots for measured dielectric constant and loss tangent as a function of frequency as reported in [27] are shown in Figure 13. A robust microwave characterization algorithm for extracting dielectric properties as well as ink conductivity was proposed in [28]. The

advantage of this approach lies in the automation of all the sub-tasks involved in modeling and optimization, facilitating an efficient parameter extraction framework. Furthermore, this algorithm

Figure 13. (a) Dielectric constant (b) Loss tangent of flexible substrates (5 mil Kapton, LCP, and PET) [27].

was able to detect the change in fabrication parameters such as change in ink conductivity due to sintering temperature variation. It was observed that losses decrease by about (40 dB/m) at 20 GHz when the sintering temperature was changed from 170°C to 220°C. Furthermore, the characteristic impedance for the inkjet printed CPWs on Kapton was extracted [28]. In [29], Kim *et al.* proposed thick and thin film processes on fabric, and their electrical characteristics were evaluated to investigate the performance and limits of the screen printing circuit technology. The ac impedance of the transmission lines were measured to be 201-215 Ω with < 7% variation, and the time-domain reflectometry profile showed that the -3 dB bandwidth of the printed transmission line of 15 cm on the fabric is 80 MHz. Furthermore, the measured resistivity, inductance, and capacitance values were found to be $5.34 \times 10^{-7} \Omega$, 970 nH, and 10 pF, respectively.

Once an optimal substrate is selected, the next task for an RFFE module design is to choose a fabrication methodology that allows integration of passive components on the substrate and the further 3D integration and stacking of individual chips from different technologies into one package (“heterogeneous integration”). In addition, to enable 5G cellular RFFEs, these fabrication methodologies should be able to support mm-wave design requirements such as low losses, high-quality factor and low-cost fabrication process. To this end, the next section discusses two novel waveguide architectures for mm-wave RF components design.

3. Recent Progress in Waveguide Architectures

The exploitation of millimeter waves for next generation mobile communications has fostered significant advances in the wireless applications at higher frequencies at 20 GHz and above. Several countries including United States, China, Japan, Sweden as well as the EU, have adopted new regulations to enable rapid development and deployment of 5G technologies from 24.5–29.5 GHz and 37–43.5 GHz [30]. All of these applications require microwave/mm-wave components to be integrated into a multilayer circuit and existing manufacturing techniques have difficulties economically achieving the required precision and they are also difficult to scale for mass production at high frequencies [31]. To address this, innovative integrated waveguides, such as the SIW [31], gap waveguide [32] have been recently proposed.

A. Gap Waveguide:

Gap waveguide technology was introduced in 2009 as an alternative to hollow waveguides and microstrip lines with performance similar to rectangular waveguides. These structures are realized using two parallel metal surfaces, one of which has a textured pattern such that there is no need for an electrical contact between the surfaces [33, 34]. A transmission line can be realized in the small gap between the two metal surfaces with the help of the texture. The wave can propagate along smooth, guiding parts such as metal ridges, grooves or strips in the textured surface [35].

In an ideal gap waveguide, there are two parallel plates, one a perfect electric conductor (PEC) and the other perfect magnetic conductor (PMC), and the guiding PEC strip is in PMC metal plate. For the waves to propagate between the plates, the air gap between the PEC and PMC plates should be greater than $\lambda/4$ [35]. It should be noted that, as PMC structures are not available in nature, they are emulated by an artificial magnetic conductor (AMC). This is usually designed with periodic textured structures such as metal pins or mushroom structures [36]. The AMC surface creates virtual lateral walls on both sides of the guiding section and thus prevents any lateral field leakage. The electromagnetic waves can then propagate along the guiding ridges, grooves, or strips. Based on the construction, the gap waveguides are referred to as ridge [37], groove [38] or microstrip gap waveguides [39]. The ridge gap waveguide, inverted microstrip gap waveguide, and microstrip-ridge gap waveguide allow a quasi-TEM mode to propagate within the stopband. In contrast, the propagating mode in the groove gap waveguide is similar to that of the TE_{10} mode of the rectangular waveguide.

Figures 14 and 15 depict the different gap waveguide configurations. An in-depth analysis of losses as well as design of parallel-plate stop-bands for various gap waveguides have been provided in [32]. One of the important advantages of the gap waveguide technology is its relatively lower losses as compared with microstrip line or coplanar waveguides at higher frequencies. This makes the gap waveguide an attractive candidate for designing mm-wave antennas for high efficiency and planar profile applications.

Figure 14. Different gap waveguide configurations (a) ridge gap waveguide (b) groove gap waveguide (c) inverted microstrip gap waveguide (d) microstrip ridge gap waveguide [32].

Several selected examples of mm-wave gap waveguide based antennas will be discussed. In [40], the authors reported the design of a 4×1 element linear slot array and a 2×2 element planar slot array antenna operating at Ku-band employing the ridge gap waveguide technology. A T-section ridge was introduced to achieve a wideband response ($>20\%$). Further, to feed the 2×2 array antenna, a compact four-way power divider was designed, where the widths of the two divided ridge sections were gradually tapered to make the impedance match. A V-band slot antenna based on ridge gap waveguide technology was reported in [41].

Figure 15. Propagating modes in different gap waveguide configurations [32].

Among all the gap waveguide topologies, groove gap waveguide offers the lowest insertion losses [32]. Hence, several antennas based on groove gap waveguide have been proposed recently, such as, untilted narrow-wall slot antenna excited by parasitic dipoles [42], single-layer cavity-backed slot array antenna [43], and leaky wave antennas [44]. Figure 16 shows the propagation constants in the designed groove gap waveguide in [42] and equivalent rectangular waveguide for hollow dimensions. It can be seen that both types of guides are pretty similar and the losses in the groove gap waveguide are very close to those of rectangular waveguide. On the contrary, microstrip gap waveguide and microstrip ridge gap waveguides are less explored topologies and have been used to design a 60 GHz quasi-planar dual-mode horn array antenna [45], and a 60 GHz planar array antenna realized on two doubled-sided PCBs using SIW cavity [46], respectively.

It is interesting to note that, the concept of gap waveguide can also be extended to a gap waveguide –based PMC packaging solution that addresses the power leakage and interference problems associated with traditional packaging technologies. This newly proposed packaging solution can be easily scaled to high frequency and shows consistent performance over frequency bands from X-band upto W-band [32].

Figure 16. Comparison of propagation constants in groove gap waveguide and rectangular waveguide of same hollow dimensions [42].

B. Substrate Integrated Waveguide:

A practical solution for mm-wave RFFE modules consists of a system-in-package (SiP) with CMOS devices integrated on a single substrate with embedded passive components. To this end, SIWs have attracted much interest as the waveguide is dielectric filled and embedded into a substrate, which can also be used for microstrip and CPW lines, lumped elements and as a chip carrier for integrated circuits [47]. SIWs were originally introduced in 1998 as laminated waveguides [67]. However, it was only in early 2000, when this technology was integrated with substrate integrated circuits (SICs), that refers to conversion of nonplanar structures like rectangular waveguide, coaxial lines etc. to planar form. SIW structures are fabricated by embedding two rows of vias or slots in a dielectric to connect top and bottom metal planes [48]. In [31], we have discussed the design principles, different loss mechanisms, and recent advances in SIW active and passive components in detail. However, a thorough literature review of SIW based diplexers is still missing. Diplexers are crucial elements of RFFE modules which impact the overall system performance [3]. The focus in this section will be to present recent developments in SIW based diplexers.

The first mm-wave SIW based diplexer was reported by Dr. Wu et al. in [49]. The diplexer was designed based on the complementary response of two dual-mode SIW circular and elliptic cavities. The measured insertion losses were 1.95 and 2.09 dB in the upper and lower passbands

centered at 26 and 25 GHz with the fractional bandwidths of 5.2% and 5.4%. A SIW diplexer based on complementary split ring resonators (CSRRs) was proposed in [50]. CSRRs are metamaterial resonators that behave as electric dipoles when excited with axial electric field. The diplexer designed in [48] offered advantages in terms of compact size, low loss, and high isolation based on CSRRs and SIW technology. Following the similar approach, a diplexer was designed on a SIW with stepped impedance complementary S-shaped resonators (CSSRs) [51]. The variable

Figure 17. (a) CSRR based diplexer proposed in [50] (b) CSRR topology (c) Stepped impedance CSRR topology as proposed in [51].

frequency response characteristics of stepped impedance resonators in this work led to a higher output isolation (> 30 dB). A SIW diplexer using dual-mode resonator was proposed in [52]. By enhancing the perturbation strength between two vias placed in the diagonal line of a square, the resonant frequencies of the dual-mode square cavity could be assigned to required frequencies. Figure 17 depicts the topology of CSRR-SIW based diplexer, CSRR structure from [50].

Very recently, several other SIW based diplexer topologies with enhanced performance were reported. Among them, in [53], a diplexer based on combline triplet sections with transmission zeros placed below and above the passband was presented. Whereas in [54], the

authors used a dual-mode cavity as a junction for designing the diplexer. The even and odd modes in this diplexer were coupled with other sections of the receiver and transmitter filters in such a way that the designed receiver and transmitter filters are independent of each other. Another dual-mode SIW based diplexer was reported in [55]. With this technique, multiple transmission zeros could be obtained on both sides of the passband for an SIW cavity, which offered a flexible design and high performance response. A novel tunable dual-mode SIW diplexer with various single-ended or balanced ports was presented in [56]. Furthermore, the SIW resonators here offered a wide tunability and low loss. A methodology for realizing compact diplexers using mixed dual-mode and single-mode resonators was presented based on an advanced coupling scheme [57]. This approach offered miniaturization compared to traditional methods since the dual-mode cavity acted as a T-junction between the input port and the two channels and provided one pole for each channel filter. One additional mm-wave diplexer was reported in [58]. Owing to the equivalence between SIW and dielectric filled waveguide (DWG), in [59] the authors presented a Ka-band diplexer that consists of a highpass filter, hybrid coupler and low-order bandpass filter. To investigate how the diplexer handles fabrication errors, the authors subjected the circuit to a tolerance analysis where simulated results suggest that the highpass filter in the diplexer is less sensitive to fabrication errors than the bandpass filter and its use in mm-wave SIW diplexer circuits can help to relax sensitivity to fabrication errors.

With the concept of SiP, one or more chip-sets can be combined in a single RFFE module with other passive components, which are fabricated with different technologies. SIW technology enables the possibility to integrate passive components, active circuits and antennas on the same substrate. Furthermore, employing SIWs, multiple chip-sets can be mounted on the same substrate, thus extending the concept of SiP to system-on-substrate (SoS). In SoS, there is no need of transitions between components fabricated with different technologies. Therefore losses and parasitics are reduced, making it an ideal platform for developing cost-effective and high-performance mm-wave RFFE modules.

4. Recent Progress in Design of multi-band passive components

Miniaturization, portability, cost and performance are the driving forces for the evolution of mm-wave applications. Therefore the next-generation RFFEs necessitate RF devices with multi-band functionality to reduce module space and cost. Among them, the power divider is a crucial component in many wireless communication systems such as Doherty power amplifiers, phased

array antennas, vector modulators, balanced mixers and frequency multipliers, antenna feeding networks, and I/Q vector modulators. In this section, a review of dual/multi-band power dividers' design will be presented. The state-of-the-art of planar dividers based on recent breakthrough, physical configurations and function integrations has already been presented in [60]. Therefore, special emphasis in our article will be given on planar dual-band Wilkinson power dividers (WPD).

The power dividers are generally used to divide the input power into smaller amounts of output powers using equal or unequal power division. WPDs were proposed in [61] with a resistive device mounted between the output ports. This power divider can imitate the properties of lossless power dividing, when all ports are matched. Later, the Gysel power divider was introduced [62] in 1975 which modified the isolation structure by introducing two grounded resistors that improve the heat dissipation performance under a high power level. The traditional WPD consists of two ($\lambda/4$) branches of transmission line and a termination resistor, where λ is the wavelength of the transmission line. These two branches match all input and output ports and the resistor provides a good isolation between the output ports for the power divider. Recently, there has been several approaches to design WPDs with better performance features such as high frequency and power division ratio. Among them one approach is to utilize open/short stubs to construct the power divider [63-65]. This approach is based on transmission lines only (except for the isolation resistors) which offers a simple structure and low loss. Furthermore, this method was able to obtain close form design equations and issues on practical impedances were also addressed. Figure 18(a) shows the design and results for WPD reported in [64]. Some other designs have topologies employing lumped R , L , and C components in their isolation networks [66-68]. This provides more flexibility in the design. For example, in [68], the odd-mode impedance was a free variable, which could be used to control the coupling between the coupled lines, as well as the values of the inductor and capacitor. However, such design have limited use at high frequencies due to inherent parasitics associated with the lumped elements. Figure 18(b) shows the design and results for WPD reported in [68]. Another solution is utilizing coupled lines [69-73]. Similar to lumped R , L , and C components method, employing coupled lines to design WPDs offer flexible design parameters due to introducing even- and odd-mode impedances. Additionally, such structures feature compact size and convenient design procedure [74].

Figure 18. WPD topologies for (a) Open/short stubs with transmission line only [64] (b) Lumped R , L , and C components [68].

Figure 19(a) depicts a design example and results of coupled line based dual band WPD [74]. Due to their unique dispersion characteristics, composite right left handed (CRLH) transmission lines have been proved as attractive candidates to design dual band WPDs. One of the most important feature of the CRLH based WPDs is that they offer significant circuit miniaturization. Figure 19(b) shows an example of CRLH based WPD topology and its results [75]. However, it is noteworthy that CLRH based power dividers suffer through inherent parasitics at high frequencies. Port matching is another simple and intuitive technique for designing WPDs which are based on the impedance matching concept [76]. However, a major limitation in the design approach in [76] was the need of an isolation resistor being a continuous function of the frequency division ratio. To address this issue, an improved port-matching technique was proposed in [77]. The improved matching criteria in this work were further able to increase the frequency division ratio. Several practical applications, such as antenna feeding networks, antenna arrays, and power amplifiers, need customized power division ratios [60]. Thus, a lot of effort from microwave community has been dedicated to design WPDs with unequal power division ratios. The first method that is widely used is the uneven-impedance method [78-81]. Here, the

characteristic impedance of the two bisections is altered to attain unequal power division. However, this method is not capable of large power division ratio because line impedances are constrained by implementable physical line widths during fabrication processes. Some other designs adopt multi-section transmission lines [82-85]. However, such designs suffer from a limited band ratio. Some of the efforts were based on Π - and T-configurations [86], [87] or coupled lines [88-90]. Moreover, although topologies utilizing R , L , and C lumped components in their isolation networks provide a higher band ratio, these designs have limited use at high frequencies due to their inherent parasitics [91, 92]. Very recently, a new methodology for the design of a dual-band unequal-split WPD with a high power division ratio (10:1) at the operating frequencies was proposed in [93]. Impractical high-impedance transmission line in the conventional divider was replaced with cascaded dual-band T-section structures to design the unequal-split WPD. Finally, a comparison between the measured responses of the proposed dual-band WPDs with some of the other state-of-the-art designs is given in Table 3.

Figure 19. WPD topologies for (a) Multi-section coupled line [74] (b) CRLH based transmission line [75].

TABLE 3
COMPARISON BETWEEN THE ELECTRICAL AND PHYSICAL CHARACTERISTICS
OF RECENT DUAL-BAND WPD DESIGNS [91]

Ref.	Applied Technique	$R=f_2/f_1$	k^2	Input/Output	Isolation	Area (mm^2)
[77]	Enhanced port	3.88	2	-16, -31	-25	—
[82]	Multi section coupled	2.50	2	-25, -20	-40	64×90
[83]	Multi section	2.68	2	-22, —	-30	60×94
[86]	Single T section with short/open stubs	1.80	2	-40, -25	-30	88×130
[87]	π -section with input/output ports	2.00	2	-20, -20	-30	53×106
[90]	Coupled lines with	1.80	7	-20, -20	-20	95×105
[92]	Lumped RLC	4.00	2	-30, -30	-30	65×240
[93]	Single/multi T-section with open stub	2.00	10	-40, -35	-40	98×131

5. Conclusion

This paper summarizes the emerging technologies for designing next generation RFFE modules. First, the primary design attributes of an RFFE module are identified. Next, in each section, pertinent examples are selected and their recent advances are discussed. Looking ahead, recent breakthroughs in substrate technologies including SOITEC's e-SI substrate, acoustic wave substrates, and flexible substrate technology are expected to offer improvements in linearity, isolation, power dissipation and per-unit-cost. Novel waveguide architectures such as gap waveguide and substrate integrated waveguide will address the constraints such as losses, power handling and packaging in mm-wave design paradigm. Finally, investigations into multiband RF components will enable replacements of multiple components with a single device, thus reducing RFFE size and power consumption. Together, these approaches propose technology options to design advanced 5G RFFE modules.

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