Using SiO₂ Carrier Confinement in Total Internal Reflection Optical Switches to Restrict Carrier Diffusion in the Guiding Layer

David Thomson, Frederic Y. Gardes, Goran Z. Mashanovich, Andrew P. Knights, and Graham T. Reed

Abstract—Total internal reflection optical switches structures are well known. However, previously reported switches based upon carrier injection have suffered from the diffusion of carriers within the guiding layer leading to inefficient reflection. While some attempts have been made to restrict the diffusion of carriers in devices fabricated in materials other than silicon, carrier diffusion has still been possible. In this paper, we propose the use of a thin SiO₂ barrier around the carrier injection region to improve the performance of the device. Modeling data has shown that high-performance switching is possible by confining the carriers in this way. Modeling suggests that switching times of the order of 5 ns can be achieved with a switching current of the order of 30 mA.

Index Terms—Carrier confinement, optical switch, silicon photonics, total internal reflection.

I. INTRODUCTION

TOTAL internal reflection optical switches based upon carrier injection have been previously reported in both silicon [1]–[5] and other semiconductor materials [6]–[9]. The advantages of such a switch over other topologies are that it can potentially be designed to be wavelength insensitive and polarization insensitive. This type of optical switch is generally of the order of an order of magnitude shorter than many other switching topologies.

The importance of having a precise controllable reflection interface in this type of switch is widely acknowledged [2]–[5], [9], and problems caused by the high injection currents required for switching have been discussed [6].

In devices fabricated in materials other than silicon, attempts have been made to confine the injected carriers to certain regions within the device to create a refractive index discontinuity and, therefore, a precise and controllable reflection interface during switching. Another motivation for using carrier confinement is to reduce the required injection current [6]–[8]. While these devices have all reported an improved performance, none of the designs show any method of lateral carrier restriction in the guiding layer itself, and, therefore, carriers are still able to

diffuse through the guiding layer freely, compromising device operation.

Thin SiO₂ layers have recently been used to form insulating boundaries in SOI-based photonic devices to form both a MOS capacitor structure in a phase modulator [10] and a carrier restrictive structure in other phase shift-based devices [11].

In this paper, the use of a SiO₂ carrier restrictive barrier in a total internal reflection-based switch is proposed to both set up a precise reflection interface and improve the carrier injection efficiency. Furthermore, since the injection region is completely isolated from the surrounding semiconductor, these devices can be packed in close proximity in switching matrices or other optical circuits without crosstalk, aiding integration, and improving the packing density, while also minimizing the injection current.

Modeling data suggests that switching times of the order of 5 ns can be achieved with a switching current of the order of 30 mA, showing improvement over previous SOI-based devices. The device is investigated in this paper for TE polarized light.

II. SWITCH DESIGN AND FABRICATION

The layout of the proposed switch is shown in Figs. 1 and 2. An example design is described to enable specific modeling to be carried out, but the design is scalable to improve switching performance. Consider a design comprising two rib waveguides of height 4 μm , width 2.8 μm , and slab height 1.77 μm intercepting at an angle θ . These rib waveguide dimensions are chosen to give both single mode performance and polarization independent propagation.

A 100-nm-deep, 1- μm -wide P-type doped region ($10^{20}/\text{cm}^3$) is located along the top of the reflection interface and a 1- μm -deep, 1- μm -wide N-type doped region ($10^{20}/\text{cm}^3$) exists at the top of the slab, with ohmic connections to an anode and cathode, respectively. These doped regions are separated by intrinsic single crystal silicon to, therefore, set up a P-i-N diode structure on one side of the reflection interface.

An aluminium layer directly on top of the rib can be problematic in terms of optical absorption. Experimental evidence has been produced to confirm that this loss is small as follows.

Rib waveguides have been produced with dimensions similar to those used for the switches. Aluminium has then been sputtered onto the surface and patterned using liftoff to leave different length strips of aluminium on different waveguides.

Fig. 3 is an optical microscope image showing a range of waveguides with different length strips of aluminium on top.

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D. Thomson, F. Y. Gardes, G. Z. Mashanovich, and G. T. Reed are with the Advanced Technology Institute, University of Surrey, Guildford, Surrey, GU2 7XH, U.K. (e-mail: d.thomson@surrey.ac.uk; f.gardes@surrey.ac.uk; g.mashanovich@surrey.ac.uk; g.reed@surrey.ac.uk).

A. P. Knights is with the Department of Engineering Physics, McMaster University, Hamilton, ON L8S 4L7, Canada (e-mail: a.knight@mcmaster.ca).

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Fig. 1. Diagram of device layout.

Fig. 2. Cross-sectional view along line XX.

Fig. 4. Excess loss caused by different lengths of aluminium.

Fig. 3. Layout of aluminium loss experiment.

Broadband light of wavelength around 1550 nm has been coupled into each waveguide and the output power measured. Fig. 4 shows the change in optical power caused by the increases in the aluminium strip length. The length of anode used in the switch is less than 100 μm . This corresponds to an optical loss of less than 0.5 dB, which is not significant.

A thin SiO₂ barrier exists along the center of the interception region and continues around a region on the side of the interception that contains the P-i-N diode to completely enclose the active region of the device. Note that away from the reflection boundary, the oxide barrier is kept normal to the direction of the propagating light to minimize the thickness of SiO₂ through which the light propagates. The SiO₂ layer extends to the buried oxide layer to, therefore, completely electrically isolate the injection region of the device.

Fig. 5. SEM images of ribs profiles produced when using different etch gas flow rates.

One proposed fabrication process is as follows. First, the thin oxide barriers are to be formed. This is done by first etching trenches through the silicon overlayer down to the buried oxide layer. The position of the edges of these trenches corresponds to the position of the SiO_2 barriers. The surface of the trenches can then be oxidized so that they have a thin SiO_2 layer on them. The trenches may then be refilled by LPCVD deposition of polysilicon and the surface planarized by using chemical mechanical polishing.

It is appreciated that polysilicon has a greater propagation loss than crystalline silicon. However, polysilicon waveguides produced by LPCVD deposition with subsequent annealing and chemical mechanical polishing have been demonstrated with losses of 34 dB/cm [12]. In this device, the light propagates through a length of approximately 100 μm , which corresponds to a loss of under 0.35 dB.

It is also appreciated that the refractive index of the deposited polysilicon and the single crystal silicon may not be perfectly match as to produce a refractive index difference on either side of the reflection interface before a forward bias is applied. Thermal processing can be used to reduce and control this difference. Further light doping or light damage formation can be used to tune the index to match that of the crystalline silicon as required.

After sample surface planarization, the rib waveguides can be formed by etching into the surface of the overlayer. Both rib and trench etches can be performed by using the Bosch RIE process. This process allows the formation of vertical sidewalls by carefully tuning the etch parameters. Experimental work has been performed to confirm that the angle of the sidewall can be controlled by adjusting the etch gas flow rate. Fig. 5 is an SEM image of rib waveguide profiles showing that when a low flow rate (50 sccm) is used a large sidewall angle is produced. As the flow rate is increased, the angle becomes smaller until it begins to slightly undercut as is the case when flow rate of 130 sccm is used (also shown). Vertical sidewalls have been repeatedly produced when a flow rate of 125 sccm is used.

Once the ribs have been formed, the doped regions can be produced via ion implantation of boron and phosphorus for the p and n type regions, respectively. Thermal annealing can be used to activate the dopants. A top SiO_2 cladding layer can be deposited via PECVD and metal contacts added by sputtering an aluminum film.

III. SWITCHING OPERATION

Under zero bias conditions, the input light propagates along the input waveguide and passes through the reflection interface to the “Transmitted” output waveguide. When the device is

forward biased, carriers are injected into, and fill the region within the inner oxide barrier perimeter. These injected carriers cause a reduction in refractive index due to the free carrier plasma dispersion effect in silicon [13]. If a sufficient refractive index change occurs, the input light will be incident on the reflection interface at an angle greater than the critical angle for total internal reflection meaning that the input light will be reflected to the “Reflected” output waveguide and, thus, switching occurs.

IV. OXIDE BARRIER

Due to its compatibility with CMOS fabrication processes, it is convenient to use SiO_2 as the barrier material. Many processes have been reported which can produce reliable SiO_2 films in the sub-3-nm regime [14]–[18].

By using ATLAS the device simulation tool from SILVACO [19], it is possible to model the effectiveness of a thin SiO_2 barrier at stopping the diffusion of carriers. Fig. 6 shows the structure used to carry out these simulations. It consists of a P-i-N diode structure with a 2-nm SiO_2 barrier, isolating the injection region of the device from a nonelectrically active region.

The carrier concentration along the YY line shown in Fig. 6 when the P-i-N diode is under a 4-V forward bias can be seen in Fig. 7. The SiO_2 barrier is at the 1 μm position on the x axis in Fig. 7. As expected, it can be seen that there is no significant diffusion of carriers through the barrier into the nonactive region, therefore demonstrating the ability to set up a refractive index discontinuity across the reflection interface.

The use of thin SiO_2 layers in the guiding layer of photonic devices has been demonstrated without it significantly perturbing the optical mode and causing significant loss [10], [11], demonstrating the feasibility of the use of such a barrier in this device. The inclusion of a 2-nm SiO_2 layer along the interception in a waveguide crossing such as that used in this work has been modeled in 2-D Fullwave, an FDTD modeling package from Rsoft [20]. Fig. 8 shows the result of this modeling. Without the barrier, a throughput power of 0.65 as normalized to the source is observed. When the barrier is included this power drops to 0.6 corresponding to an excess loss less than 0.35 dB. For this reason, and to ease computational effort the barrier has been omitted from further optical simulations.

V. MODELING EVIDENCE

Optical modeling of this device has been carried out using BeamProp, a modeling package from Rsoft based upon the beam propagation method [20]. The distribution and concentration of the injected carriers under forward bias is modeled in ATLAS. The structures used to model the device are exactly as within the SiO_2 barrier shown in Figs. 1 and 2.

Fig. 9 shows the electron concentration along the reflection interface while the device is under forward bias. A similar concentration is observed for holes. The electron concentration varies by approximately 1% along the reflection interface so one representative point can be probed for use in the model without introducing significant error. The carrier concentration at this point has then been used to represent the carrier concentration along the entire reflection interface under different bias

Fig. 6. Diagram of the structure used to model the insulating effectiveness of the SiO₂ barrier.

Fig. 7. Carrier diffusion through barrier.

conditions. The free carrier concentration has been converted to changes in refractive index and absorption using the expressions (1) and (2) produced by Soref and Bennett in [13]

$$\begin{aligned} \Delta n &= \Delta n_e + \Delta n_h \\ &= - \left[(8.8 \times 10^{-22} \Delta N_e) + (8.5 \times 10^{-18} (\Delta N_h)^{0.8}) \right] \end{aligned} \quad (1)$$

$$\begin{aligned} \Delta \alpha &= \Delta \alpha_e + \Delta \alpha_h \\ &= 8.5 \times 10^{-18} \Delta N_e + 6.0 \times 10^{-18} \Delta N_h. \end{aligned} \quad (2)$$

By using these expressions, the optical and electrical modeling can be linked together to analyze the optical behaviour of the device under forward bias conditions. Some of the important parameters used in the simulations are given in Table I, along with the references from which the values are obtained where applicable.

It is desirable to minimize the crosstalk between the output waveguides of any type of optical switch, in both the switched and unswitched states. Crosstalk has been defined in this work as shown in (3) and (4) for the switched (X_S) and unswitched (X_U) state, respectively

$$X_S = 10 \log \left(\frac{P_t}{P_r} \right) \quad (3)$$

$$X_U = 10 \log \left(\frac{P_r}{P_t} \right). \quad (4)$$

P_t and P_r are optical powers in the transmitted and reflected output waveguides respectively, normalized to the power coupled into the input waveguide. Waveguide crossings such as those used in the switch of this work have been shown to exhibit large crosstalk values when the interception angle between the waveguides becomes small [23]. This is supported by the results of optical modeling carried out in this work as shown in Fig. 10.

Fig. 10 shows that, in order to obtain low crosstalk figures, large interception angles are required. At larger interception angles the magnitude of the refractive index variation, and, therefore, the carrier injection required for switching becomes very large (roughly 1.5×10^{19} for a half interception angle of three degrees). This leads to larger switching currents and slower switching speeds. The problem can be overcome by tapering the waveguide width outwards as it approaches the interception region. A parameter called the taper factor has been defined as the waveguide width in the center of the interception region divided by the original width, tapering over a 100 μm propagation length. Fig. 10 also shows the crosstalk in the unswitched state for taper factors 1.4, 1.8, and 2.2 across a range of half interception angles. It can be seen that low crosstalk figures can be achieved at small interception angles if large taper factors are used.

The crosstalk with an applied forward bias of 1.5 V for taper factors 1.4, 1.8, and 2.2 can be seen over a range of half interception angles in Fig. 11.

No significant taper factor dependence can be seen in the crosstalk figure in the switched state indicating that no detrimental effects have been produced here by using tapered waveguides.

Modeling has demonstrated that as the drive current is increased (due to increasing forward bias), the power at the output of the “transmitted” waveguide decreases while the power at the output of the “reflected” waveguide increases. The switching current can be calculated as the drive current required for the power in the “reflected” output waveguide to reach 90% of its maximum value. Fig. 12 shows the angle and taper factor dependence on the switching current.

Fig. 12 demonstrates that as the interception angle of the waveguides increases the required switching current also increases. This is because a larger refractive index change is required since light is incident on the reflection interface at a smaller angle.

The rise time has been calculated as the time required for power at the output of the “reflected” output waveguide to rise

Fig. 8. Two-dimensional FDTD modeling of the propagation of light through device (a) with 2-nm SiO_2 layer and (b) without SiO_2 layer.

from 10% to 90% of its maximum value upon the application of a 1.5-V forward bias. Likewise, the fall time is the time required for the power in the “reflected” output waveguide to fall from 90% to 10% of its maximum value with this forward bias removed. The rise and fall times can be seen in Fig. 13 for a range of taper factors and interception angles.

VI. SUMMARY OF MODELING RESULTS

Observing the results obtained for switch with a 1.5° half interception angle and 2.2 taper factor it can be seen that the

Fig. 9. Carrier concentration along reflection interface.

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Wavelength	1.55 μm
Hole carrier lifetime	300 ns [21]
Electron carrier lifetime	700 ns [21]
Surface Recombination Velocity	200 cm/s [22]

Fig. 10. Crosstalk in the unswitched state for different taper factors over a range of half interception angles.

crosstalk in the switched and unswitched states are approximately -17 and -12 dB, respectively (Figs. 10 and 11). Rise and fall times of approximately 2 and 5 ns are demonstrated (Fig. 13), and a 30-mA switching current is required (Fig. 12). These results show a considerable performance improvement over other SOI-based total internal reflection-based switches from the literature which do not have carrier restriction. For example, the device in [5] has a switching time of 110 ns and a switching current of 60 mA, values that are by factors of 22 and

Fig. 11. Crosstalk in the switched state for different taper factors over a range of half interception angles.

Fig. 12. Switching current required for different interception angles and taper factors.

2, respectively, larger than the switching time and switching current in our device. The interaction length (length of the reflection interface) in [5] is 190 μm compared to 134 μm in our device, showing a reduction in the use of the material. The crosstalk in either state is not mentioned in [5]; hence, it is not possible to compare the two devices in that respect. It is appreciated in these comparisons, however, that these device dimensions differ to those in the literature (8- μm waveguide height and width used in [5]). An optical switching device of this type would be suitable for applications in low cost networks, and short point to point networks in the future that are less demanding.

VII. CONCLUSION

A total internal reflection-based optical switch has been proposed in silicon-on-insulator with a SiO₂ carrier restrictive boundary to create a precise reflection interface and improve carrier injection efficiency. The SiO₂ barrier will also mean that integration will be aided and packing density improved

Fig. 13. Rise time and fall time for different interception angles and taper factors.

since these devices can be packed in close together without interfering with one other. Modeling results have shown that for an example device the switching current is 30 mA and switching time 5 ns, demonstrating that high performance switching can be achieved with this type of switch.

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David Thomson has been a Researcher in the field of silicon photonics since late 2004 when he joined Prof. G. T. Reed's research group as a Ph.D. student at the University of Surrey, U.K. Prior to that, he studied electronic engineering, also at the University of Surrey, and graduated with first class honors.

Frederic Y. Gardes received the DUT in physics measures from the University of Rennes, France, the B.Sc. degree in applied physics from the University of Portsmouth, U.K., and the M.Sc. degree in optoelectronic and communication systems from Northumbria University, U.K. He is currently pursuing the Ph.D. degree at the University of Surrey, U.K., where he is studying with the Silicon Photonics Research Group under the supervision of Prof. G. T. Reed.

Goran Z. Mashanovich received the Dipl. Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, and the Ph.D. degree from the University of Surrey, U.K.

After working for five years as a Teaching and Research Assistant at the Faculty of Electrical Engineering, University of Belgrade, he joined the Silicon Photonics Group at the University of Surrey in 2000. Since 2006, he has been the Group Manager.

Andrew P. Knights received the Ph.D. degree from the University of East Anglia, U.K., in 1994, following work on the interaction of slow positrons and electrons with solid surfaces.

Following a postdoctoral appointment at the University of Western Ontario, London, ON, Canada, he joined the University of Surrey Ion Beam Centre, U.K., in 1997, where he developed processing strategies for the application of ion beams in micro- and opto-electronics. From 2000 to 2003, he was a Principal Engineer at Bookham Technology as part of the team which brought to market the first silicon photonic devices. Since 2003, he has led a research group at McMaster University, Hamilton, ON, in the integration of photonic and electronic functionality on a silicon platform.

Graham T. Reed has been active in research in guided wave optics since approximately 1983, and in May 1989, he joined the University of Surrey, U.K., where he formed the Silicon Photonics Research Group. He was the principal author of the first textbook on silicon photonics, has authored five further book chapters in other publications, and published over 200 papers.

Prof. Reed is a member of three international conference committees related to silicon photonics, and Co-Chair of the Silicon Photonics Symposium that is part of Photonics West, held annually in San Jose, CA, one of the largest annual photonics meetings.