Micron-scale inkjet-assisted digital lithography for large-area flexible electronics

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Abstract— Large-area electronics require cost-effective yet precise patterning of electrodes. We demonstrate a simple electrode patterning technique capable of micron-scale gap formation, that allows the patterning of a larger variety of metals than the current portfolio of jettable metallic ink comprises and does not require a high-temperature sintering step. However, this method can produce large variations in gap size resulting in inconsistent and irreproducible transistor drain current. We propose that source-gated transistors (SGTs) are well suited to this technique, as they have a saturated drain current independent of source-drain separation, thus leading to improved current uniformity despite inconsistencies in gap size.

I. INTRODUCTION

The principal advantages of large-area electronic circuits made by solution processing [1] are cost-effectiveness and production volume. Inexpensive materials and low temperature processing allow for significant cost savings when compared to conventional techniques, while the use of a flexible substrate enables economic roll-to-roll production.

Device-to-device current uniformity over a large area is still difficult to attain due to factors such as the randomness inherent in material crystallization [2], bias- and temperature-dependent mobility [3], contact effects [4,5] and moisture- or oxygen-related instability [6]. Of great consequence to applications are also the resolution and repeatability of patterning by large-area techniques.

In this paper we show how an augmented version of digital lithography by inkjet printing [7] can be used to realize small gaps between electrodes such as micron-scales source-drain gaps for source-gated transistors which have a uniform current regardless of the source-drain separation [8]. Owing to their operation and with proper design, these transistors could be used in solution-processed large-area circuits where matching of current between devices, low voltage operation and, high intrinsic gain, are required. The method applies equally to patterning micron-scale gaps between conductive traces for other large-area applications such as large area photovoltaics and light sources.

II. FABRICATION OF ELECTRODES AND TRANSISTORS

A. Electrode patterning by inkjet printing and etching

Inkjet printing represents a promising technique for field-effect transistor (FET) fabrication [5]. Metallic nanoparticle inks allow patterning of high-conductivity traces as electrodes for transistors. However, high-temperature ink sintering, poor repeatability and the necessity to pre-treat the substrate for improving resolution are aspects which complicate the fabrication of short-channel, integrated transistor arrays on large substrates.

Here we extend the method of patterning electrodes by digital lithography [7] through the addition of several low-temperature steps. Figure 1 shows the process flowchart.

Figure 1. Flowchart of fabrication steps for conductive (here metallic) electrodes with micron-scale gaps by inkjet printing.

The pattern is drawn on the metal-coated substrate by inkjet printing a material which serves as an etch barrier. The metal is subsequently etched for a period of time which allows for etch-back to occur. With the barrier layer still in place, the second metallic layer is deposited to form the second electrode. Finally, the gap between the two metals is revealed by lifting off the barrier layer.

We have found poly (methyl methacrylate) (PMMA) to be an excellent barrier material for etching Au and adequate for etching Cr, Cu and Ag. To print PMMA patterns, an ink was created by dissolving PMMA in 1-Methyl-2-pyrrolidinone (NMP) stirred for several hours at 50°C. We chose NMP for its high boiling point (202°C) and suitable surface tension for piezoelectric jetting. Possible substitute inks (which were not investigated) are PMMA in anisole or γ -butyrolactone, polystyrene (PS) in toluene or diethyl phthalate, or conventional photoresists diluted to allow jetting.

Unlike photoresist, our PMMA ink does not require UV curing or a high-temperature bake. The best results are obtained with the DMP-2800 printer and DMC-11610 cartridge using: 2-5% PMMA concentration in NMP, nozzles held at room temperature, platen temperature of 50°C, jetting voltage of 25-35V, drop spacing of 35 μ m and printing with one to three adjacent nozzles in one to six layers. Fabrication and characterization using a Keithley 2400-based system have been performed in air at room temperature.

The main advantages of the technique are: a larger range of conductors can be patterned by this method, as the choice of conductive inks for printing is limited; potentially, no requirement for a high-temperature sintering step; the ability to create gaps which are far less than the minimum line width achievable by conventional inkjet printing.

Figure 2 represents images of the printed PMMA trace on gold (a) and the gaps (b, black lines) which can be obtained by the technique described. Figure 2 (c) shows that poor jetting quality or imperfections of the substrate can greatly reduce the edge quality of the inkjet-printed line, yet the gap (in black) is present, with no short circuits. Sub-micron gaps can be obtained with this technique, as shown by Figure 2 (e). Increasing the etching time (Figure 1) changes the average width of the gap (Figure 2 (f)). This experiment simulates effects most likely obtained on a large substrate, for which both first-metal thickness and etch rate may vary from the center to the edge and could result in gap size variations. It is unlikely that field-effect transistors (FETs) with reproducible current can be made on a large substrate with this technique.

However, source-gated transistors (SGTs) are ideal structures for this process, as their current is independent of gross fluctuations in their source-drain gap. Source-gated transistors (SGTs) [8] are field-effect transistors which differ from standard FETs in two aspects. Firstly, the source contact comprises a potential barrier and the semiconductor can be depleted by this reverse-biased barrier; secondly, the gate electrode overlaps the source and is located on the opposite side of the semiconductor.

Figure 2. Micrographs of: a) inkjet printed PMMA line on gold, showing the minimum line width attainable (approx. 40 μ m); b) micron-scale gaps obtained by etch-back, significantly smaller than the minimum printed line width; c) poor-quality printed line with irregular edges but reliable gap with no short-circuits; d) ragged edge of a $\sim$ 5 μ m gap at high magnification; e) AFM image of a sub-micron gap between gold and silver electrodes; f) Etching time affects the size of the gap (black lines) between electrodes.

In a sense, the SGT is an FET with parasitic elements, and it is very likely that a great proportion of staggered-electrode organic TFTs are in fact SGTs. As we have shown in the past [9], SGT properties which appear to be downsides (source-gate overlap and current limited by the source barrier) lead to behavior which can be exploited to create devices with improved gain, large-area uniformity and power efficiency. With proper design, the current is exclusively controlled by the reverse-biased source barrier. The role of the overlapping gate is to control the magnitude of the current either by modulating the barrier height [8] or by restricting the current under the reverse-biased barrier depletion layer [5, 10].

In practice, owing to common metal work functions and organic semiconductor ionization potentials (IPs), a Schottky barrier is almost always present at the contacts [4]. Moreover, staggered structures are seldom self-aligned, so an overlap between source and gate exists [5]. For these reasons, the fabrication of organic source-gated transistors (OSGTs) is to some extent an even simpler process than that of ohmic-contact FETs.

SGTs could be used as building-blocks for inexpensive yet high-uniformity, solution-processed analog and mixed signal circuits. To illustrate the insensitivity of SGT drain current to source-drain gap we plot output current versus source-drain gap in polysilicon devices (Figure 3(a), technology described

in [9]) and bottom-contact top-gate organic transistors made with ADS250BE and Cr electrodes (Figure 3(b)).

As can be seen, the current is practically independent of large variations in source-drain gap. Devices of this type are expected to function well and with the same “on” drain current for a given gate bias if fabricated with the etch-back / lift-off technique we present here. The alignment or definition of the gate electrode is not critical [11] and inkjet printed gates can be used even when the quality of the printed lines is sub-optimal.

B. Organic transistor fabrication

Using the technique presented we have fabricated a first batch of transistors on flexible, transparent Teonex® polyethylene naphthalate (PEN) substrates 125 μ m thick, to serve a proof of concept. Figure 4 shows schematically the structure of the transistors, while Figure 5 illustrates the flexible substrate during processing and the finished devices. Optical microscope images in Figure 6 show the position of electrodes, the suboptimal quality of the printed gate electrode and the size of the gap between source and drain electrodes.

Au bottom contact thickness was 90nm for the first metal layer and 35nm for the second, both deposited by sputtering over 2nm Ti for improved adhesion. A thicker first metal was used to aid the lift-off process.

Figure 3. Measured relative drain current against source drain gaps for several polysilicon SGTs with $W = 50 \mu$ m and biased around $I_D = 2 \mu$ A (a) and OSGTs made with ADS250BE and Cr bottom contacts (b); the FET model predicts a $1/L$ dependence of drain current, while the SGT drain current is insensitive to large changes of source-drain gap.

Figure 4. Schematic cross-section and b) top view of the fabricated devices, showing source-gate overlap (S), source-drain gap (d) and device width (W).

Figure 5. Photo- and micrograph of flexible substrate containing an array of structures; top: view of substrate with electrodes; bottom: finished devices.

Figure 6. Optical micrographs of the transistor structures, showing relative position of electrodes, the rough patterning of the inkjet printed gate electrode and size of source-drain gap obtained by etch-back and lift-off.

Etching of the first metal was done at room temperature by immersion in a solution of $KI:I_2:H_2O$ in 4:1:80 proportion for 150 seconds. The electrodes were oxygen-plasma cleaned at 100W for 5 minutes, then treated with perfluorobenzenethiol (PFBT) (Aldrich, $5 \times 10^{-3} \text{ mol} \cdot \text{L}^{-1}$ solution in ethanol) for 15 min and washed with ethanol. 35nm of small molecule semiconductor ($\mu=0.03$) was spun from solution at room temperature to form the semiconductor as per [12] and baked at 90°C for 10 minutes. A top layer of Cytop CTL-809M (9%, as received) $\sim 2 \mu$ m thick was used as the gate dielectric. Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) gates were inkjet-printed on Fujifilm Dimatix DMP-2800 (CLEVIOS™ P Jet HC commercial ink, 24 V, 15 μ m drop spacing, 3 layers for 170 nm thickness, room temperature) after oxygen-plasma treating the Cytop at 70W for 2 minutes in order to reduce surface hydrophobicity.

III. ELECTRICAL MEASUREMENTS AND DISCUSSION

We have performed initial electrical measurements on several structures. With the exception of a few short-circuited bottom electrodes due to stray satellite droplets during

printing, the reliability is very high.

Figure 7 shows the output characteristics of a typical device in which the source was the first (thicker) metal, together with the output conductance calculated from the same data. Transistor width was approximately $W = 300\mu\text{m}$. While gate leakage, on-off ratio and saturation are comparatively poor, these initial measurements show that the technique can be successfully applied for making transistor electrodes. In principle, there is no reason why the technique could not produce, with optimization, state-of-the-art devices.

In SGTs the voltage at which saturation occurs through source pinch-off (V_{SATI}) according to the dielectric model [8]. Given our process parameters, we calculate the change in V_{SATI} with V_G is roughly $0.03 - 0.05$, significantly smaller than 1, which is the case for conventional ohmic-contact FETs and in accordance to what is observed from Figure 7. Because of the very poor saturation behavior of this test device which can hardly be appreciated from the output curves, we use the output conductance (g_d) as a convenient graphical means of roughly estimating V_{SATI} . g_d clearly shows a minimum in the region of V_D where saturation is expected to happen, yielding dV_{SATI} / dV_G of approx. 0.04. We explain the poor saturation of this particular device by the fact that the source-drain gap ($\sim 2.5\mu\text{m}$) is small compared to the gate insulator thickness ($2\mu\text{m}$) and so the effect of drain electric field on the edge of the source [5, 9] is as pronounced as that of gate-induced field. Certainly with thinner insulators and geometry optimization the characteristics can be made to resemble typical SGT output curves with high output impedance above V_{SATI} and low saturation voltage for improved power efficiency and amplification ability when compared to conventional TFT structures of the same geometry [9].

The test device also has high leakage current so the transfer characteristic (not shown) is poor. Usually, the off current is dominated by the FET channel and SGT operation does not bring any detriments to the subthreshold region, particularly as short channel effects can be reduced through choosing the correct operating mode by design [10].

Figure 7. Measured output characteristics and output conductance, showing the early saturation (here $V_{\text{SATI}} < 2\text{V}$) expected of source-gated transistors according to Shannon and Gerstner's dielectric model [8]. $W \approx 300\mu\text{m}$.

IV. CONCLUSIONS

We have presented a variation of the inkjet-assisted digital lithography technique for patterning electrodes with a wider choice of metals than is possible by direct jet printing of metallic inks. Additionally, the process does not require sintering at high temperature and permits realizing reliably smaller gaps than the minimum line spacing of the printer.

The electrode gap obtained is prone to variations which are not negligible and make the method, in principle, difficult to apply to uniform FET fabrication over a large surface area.

Source-gated transistors (SGTs) have a different current control mechanism to regular FETs and are very tolerant to gap variations and well suited to our patterning method.

We believe that source-gated transistors (SGTs) are robust building blocks for large-area electronic circuits which require good uniformity of drain current, low saturation voltage [5, 8] and potentially high intrinsic gain [9]. Analog and mixed signal applications on large flexible substrates could benefit from integrating this type of device.

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REFERENCES

- [1] G. H. Gelinck et al., "Flexible active-matrix displays and shift registers based on solution-processed organic transistors", *Nature Materials*, vol. 3, pp. 106 – 110, 2004.
- [2] J. A. Lim, H. S. Lee, W. H. Lee, K. Cho, "Control of the Morphology and Structural Development of Solution-Processed Functionalized Acenes for High-Performance Organic Transistors", *Adv. Functional Mat.*, vol. 19 (10), pp 1515 – 1525, 2009.
- [3] M. Matters, D.M. de Leeuw, P.T. Herwig, A.R. Brown, "Bias-stress induced instability of organic thin film transistors", *Synthetic Metals*, vol. 102 (1 – 3), pp. 998 – 999, 1999.
- [4] H. Klauk et al., "Contact resistance in organic thin film transistors", *Solid-State Electronics*, vol. 47 (2), pp. 297 – 301, 2003.
- [5] M. Rapisarda et al., "Analysis of contact effects in fully printed p-channel organic thin film transistors", *Organic Electronics*, vol. 13, pp. 2017 – 2027, 2012.
- [6] D. Li, E.-J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. Bao, "Humidity effect on electrical performance of organic thin-film transistors", *Appl. Phys. Lett.*, vol. 86, p. 042105, 2005.
- [7] W. S. Wong, S. E. Ready, J.-P. Lu, and R. A. Street, "Hydrogenated Amorphous Silicon Thin-Film Transistor Arrays Fabricated by Digital Lithography", *IEEE Electron Dev Lett.*, vol. 24 (9), pp. 577–579, 2003.
- [8] J. M. Shannon and E. G. Gerstner, "Source-Gated Transistors in Hydrogenated Amorphous Silicon", *Solid-State Electronics*, vol. 48 (6), pp. 1155 – 1161, 2004.
- [9] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, "Intrinsic Gain in Self-Aligned Polysilicon Source-Gated Transistors", *IEEE Trans. Electron Devices*, vol. 57 (10), pp. 2434 – 2439, 2010.
- [10] J. M. Shannon et al., "Low-field behaviour of source-gated transistors", accepted for publication in *IEEE Trans. Electron Devices*, vol. 60, doi: 10.1109/TED.2013.2264547, 2013.
- [11] R. A. Sporea, X. Guo, J. M. Shannon, and S. R. P. Silva, "Effects of process variations on the current in Schottky Barrier Source-Gated Transistors", *Proc. CAS 2009*, pp. 413 – 416, 2009.
- [12] S. Georgakopoulos, D. Sparrowe, F. Meyer, M. Shkunov, "Stability of top- and bottom-gate amorphous polymer field-effect transistors", *Appl. Phys. Lett.*, vol. 97, p. 243507, 2010.