Performance trade-offs in polysilicon source-gated transistors

**R. A. Sporea¹, M. J. Trainor², N. D. Young³, X. Guo⁴,
J. M. Shannon¹ and S. R. P. Silva¹**

¹Advanced Technology Institute
University of Surrey
Guildford, Surrey, GU2 7XH, U.K
r.a.sporea@surrey.ac.uk
[+ 44 \(0\) 1483 68 9859](tel:+441483689859)

²MiPlaza, Philips Research
High Tech Campus 4
5656 AE Eindhoven, The Netherlands
mike.trainor@philips.com

³Philips Research
101 Cambridge Science Park, Milton Road
Cambridge CB4 0FY, U.K
nigel.young@philips.com

⁴Displays and Lighting Centre,
Shanghai Jiao Tong University,
Shanghai, 200240, China
x.guo@sjtu.edu.cn

Abstract—Self-aligned Schottky-source source-gated transistors (SGTs) have been made in polysilicon. The structures enable a direct comparison to be made between a SGT and a standard thin-film field-effect transistor (FET) on the same device. SGTs having excellent characteristics have been fabricated, with intrinsic gains approaching 10,000. The effects of bulk doping in the polysilicon and of the source barrier modification implant are considered in the context of the electrical output characteristics. It is shown that the choice of source length is a tradeoff between device speed and variations in current output due to variability during fabrication.

Keywords—Source-gated transistor, thin-film transistor, analog circuits, Schottky barrier, intrinsic gain.

1. INTRODUCTION

Source-gated transistors (SGTs) operate using the field dependence of the current through a reverse biased source barrier. As such, their characteristics and properties are very different from those of thin-film field effect transistors (FETs). In this paper we report measurements and modeling on SGTs in polysilicon and show the well known advantages of the SGT compared to standard FETs, namely high output impedance and low saturation voltage [1, 2]. The kink effect [3] due to bipolar amplification of carriers generated in the high field regions around the drain is absent, postulated as a result of minority carrier extraction by the reverse biased source barrier.

In this paper, special attention is given to how the electrical characteristics and intrinsic gain depend on the doping of the polysilicon and on the barrier modification implant. There is some consideration of how source length affects current density and frequency response. We also introduce the hybrid mode of operation in which the current is influenced by the parasitic FET in series with the source barrier. It is suggested that this mode of operation can explain the very low temperature dependence of the drain current measured in some devices. These polysilicon SGTs are particularly relevant to high performance thin-film analog circuits.

Source-gated transistors were fabricated in polysilicon on a glass substrate using back exposure and ion implantation to align a bottom gate with ohmic drain contacts on

either side of a Schottky source barrier. A micrograph of one of the devices is shown in Fig. 1. A 40nm layer of polysilicon was formed on top of 200nm SiN_x plus 200nm SiO₂ using a 308nm XeCl excimer laser. The Schottky source barrier was realised via a window in 120nm of SiO₂ and was modified using low energy implants of either P or BF₂. The chromium was extended over the oxide to form a field plate structure to provide field relief at the edge of the source (Fig. 2).

2. RESULTS AND DISCUSSION

2. 1. *Effect of bulk doping on SGT and FET characteristics*

In source-gated transistors the drain contact is forward biased in the on-state. As such, it can comprise a potential barrier just like the source and the source and drain can therefore be reversed to give symmetrical SGT characteristics. In the structure considered here, however, the drain contact is ohmic; therefore, if we swap the source and drain contacts we get a completely different characteristic (that of a FET with an ohmic source and a forward biased Schottky barrier at the drain). This asymmetry allows the characteristics of a SGT to be compared directly to those of a similar FET on the same device. An example is shown in Fig. 3.

The high output impedance and the low saturation voltage of the SGT are apparent, as is the kink effect in the FET. It is also seen that the FET does not switch off as well as the SGT. The off-current of the FET increases with n-type doping in the polysilicon (Fig. 4) but we see that the off-current of the SGT is always the same independent of doping. This is because the reverse biased source barrier of the SGT blocks current flow through the polysilicon between source and drain. The on-current through the SGT depends on the choice of source barrier height.

2. 2. *Effect of barrier modifying implants*

Low energy BF₂ or P implants into the source window were made before metallization in order to affect the Schottky barrier height. The transfer curves (Fig. 5) are consistent with an increase in barrier height for p-type doping and a decrease for n-type doping, as expected from barrier modification theory [4]. However, the changes in

current are small when considering the doses used, which suggests poor electrical activity. This is not surprising, because the annealing temperature was only 500°C to avoid glass compaction. All transistors showed SGT behaviour, even those with the highest n-type implants. As can be seen, the current handling of the SGT can approach that of a FET having the same geometry by tailoring the source barrier. Also, changing the source barrier height has no effect on the off-current; on to off ratios can be more than 6 orders of magnitude.

2. 3. *Effect of bulk doping and barrier modifying implants on intrinsic gain*

The high output impedance of the SGT makes it very useful for analog circuits. A key parameter in this context is the intrinsic gain, g_m/g_d . The high impedance arises because the device first pinches off at the source (at $V_D=V_{SAT1}$), and then at the drain, as in a conventional FET (at $V_D=V_{SAT2}$). [5]

Fig. 6 shows measured intrinsic gains for identical devices but for different n-type doping levels in the polysilicon. Peak gains are very high, approaching 10,000. The peaks in the curves tend to be associated with V_{SAT1} and V_{SAT2} [5] while the falloff in gain at high V_D is related to an increase in g_d due to carrier generation in the high field regions at the drain end of the device.

It is seen that the gain at low V_D around V_{SAT1} increases with decreasing substrate doping levels. This can be explained by an increase in the electric field at the periphery of the source as V_D increases and the depletion layer expands towards the drain. For higher doping levels in the polysilicon, the increase in electric field will be greater, as will the increase in g_d . At higher V_D , however, gains are greatest for higher substrate doping. Since g_m is the same, this effect must be due to carrier generation in the high field regions.

Overall, the gain envelope over V_D is highest for the more lightly doped polysilicon and gain variations with V_D are due to changes in the output conductance.

In Fig. 7, intrinsic gains are shown for two transistors with the same doping level in the polysilicon but with different barrier modification implants. Both are operating at the same current, but g_m in (a) is larger than in (b) (see Fig. 5), which explains its higher intrinsic gain. In this case, while the peaks and the dips are due to changes in g_d , the downward shift of (b) relative to (a) results from a change in g_m . For comparison,

the intrinsic gain of the FET is ~ 10 .

2. 4. *Effect of source length on current density*

The change of current with source length (S) has been measured in the past and it has been shown that the current is concentrated at the edge of the source as shown in Fig. 2. This has important implications because calculations show [6] that the cutoff frequency (f_T) of the SGT is proportional to the average current density (J_S) passing through the source. Fig. 8 depicts the results of computer simulations of drain current obtained for a given bias and over a range of source lengths. The simulation was performed using Silvaco Atlas with standard polysilicon material models, default parameters for the Schottky contact model with surface recombination and a barrier lowering constant of 3nm. Fig 8(a) shows that, as source length increases, the drain current saturates (S_{SAT}). Therefore, increasing S reduces J_S , since the current becomes almost independent of S .

If high f_T is required, the source should be less than S_{SAT} ; if consistency of current output from multiple devices is needed, however, S should be greater than S_{SAT} . The current mismatch between two devices with a change of $0.1\mu\text{m}$ in source length is shown in Fig. 8(b). As the source length is reduced below S_{SAT} the current density, and implicitly f_T , can be greatly increased, but at the same time the difference in current between two slightly mismatched devices rises rapidly. Thus, a trade-off needs to be made between the speed of the device and the desired repeatability of performance across devices, chips and lots.

2. 5. *Hybrid operation and the temperature dependence of drain current*

One parameter that should be worse in a Schottky source SGT compared with an FET is the temperature dependence of the current. Since there is a barrier at the source, the current is thermally activated. Although activation energy measurements show that we are able to pull barriers down to less than 100meV, this is still larger than that measured in a polysilicon FET [7]. One way of reducing the temperature coefficient would be to make a thermionic emission source in which, under bias, carriers would tunnel through the barrier at the Fermi level of the metal [8]. This structure would require careful engineering using thin insulating layers and doping profiles.

We have measured SGT devices where the activation energy falls to very low values

with increasing V_G and it was observed that devices with low activation energies operated at the highest currents and there was an increase in V_{SAT1} .

The output characteristic of one such device is shown in Fig. 9. The change in drain current between 33°C and 60°C is <10%. Since no deliberate attempt had been made to make a field emission source, it seems unlikely that the low activation energy is due to the source, but it is possible. From this figure we can extract the activation energy graph (Fig. 10) which shows a lowering of the curves' slope as gate voltage increases. A clearer representation is shown in Fig. 11, which describes the change of activation energy with gate bias. The curve (Fig. 11b) corresponds to the device in Figs. 9 and 10, and shows the modulation of the activation energy by gate field, together with the very low values which can be obtained. This curve is contrasted to that generated by a high-barrier Schottky-source SGT (Fig. 11a) in which the source barrier is pulled down by the gate but remains high.

Fig. 9 also indicates that for this device dV_{SAT1}/dV_G is ~ 0.4 which while being less than half that of a FET is greater than that expected from a SGT of this geometry. The increase in V_{SAT1} can be explained if a proportion of V_D is dropped across the parasitic FET. In this case saturation occurs at a higher V_D because the voltage drop in the parasitic FET is in series with that dropped across the source barrier. We conclude, therefore, that these devices operate in a hybrid mode in which the on-state is partly controlled by the source barrier and partly by the parasitic FET. It seems that there is a negative feedback effect in which the FET, with its very low activation energy of the current restricts the change of current through the source. This hybrid mode could be very important when small changes of current with temperature are required. The tradeoff is a small increase in V_{SAT1} . To fully understand the interaction between the source barrier and the parasitic FET in this situation requires a further 2D numerical analysis.

3. CONCLUSIONS

Self-aligned polysilicon SGTs have been fabricated. Measurements show an absence of the kink effect responsible for degrading the output characteristics of polysilicon FETs. Output impedances are very high, in some cases resulting in intrinsic gains

approaching 10,000. While a FET cannot be switched off when the semiconductor is highly doped, an SGT can always be switched off and the off-current is independent of doping level. The intrinsic gain envelope is broader for higher substrate doping but the highest gains were observed with the lowest doping. It is shown that the choice of source length is a tradeoff between speed and current uniformity. Some high current transistors with SGT characteristics have very low activation energies. We attribute this behaviour to a hybrid mode of operation. It has been shown that there are a number of options and tradeoffs which should enable high performance digital and analog circuits to be made in polysilicon.

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REFERENCES

- [1] J. M. Shannon and E. G. Gerstner, *IEEE Electron Dev. Lett.*, 24, no. 6, pp. 405-407, 2003.
- [2] J. M. Shannon and E. G. Gerstner, *Solid-State Electronics*, Vol. 48, No. 6, pp. 1155-1161, 2004.
- [3] A. Valletta, P. Gaucci, L. Mariucci, G. Fortunato and S. D. Brotherton, *Appl Phys Lett*, vol. 85, no. 15, pp. 3113-3115, 2004.
- [4] S. M. Sze, “Physics of semiconductor devices”, Second Edition, *John Wiley & Sons*, 1981.
- [5] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, *IEEE Trans. Electron. Devices*, vol. 57, iss. 10, Oct. 2010.
- [6] J. M. Shannon and F. Balon, *IEEE Trans. Electron Devices*, Vol. 56, Issue 10, pp. 2354-2356, 2009.
- [7] Y. Morimoto, Y. Jinno, K. Hirai, H. Ogata, T. Yamada, and K. Yoneda, *J. Electrochem. Soc.*, Vol. 144, Issue 7, pp. 2495-2501, 1997.
- [8] J. M. Shannon and F. Balon, *Papers from ITC'07, Solid State Electronics*, Vol. 52, pp. 449 – 454, 2008.

Fig. 1. Micrograph of a self-aligned polysilicon SGT.

Fig. 2. Schematic cross-section of a self-aligned SGT showing current crowding at the edge of the source.

Fig. 3. Characteristics of SGT (a), (b) and FET (c), (d) behaviour, at a similar current, obtained by interchanging the source and the drain on the same device. $W=50\mu m$, $S=8\mu m$, $d=10\mu m$, $1 \cdot 10^{13}/cm^2$ BF_2 barrier modification implant.

Fig. 4. Transfer curves of SGTs and FETs for different substrate dopings. $W=50\mu\text{m}$, $S=8\mu\text{m}$, $d=10\mu\text{m}$, $1 \cdot 10^{13}$ BF_2 barrier modification implant; areal substrate doping: a) $0.5 \cdot 10^{12}$, b) $1.5 \cdot 10^{12}$, c) $2.5 \cdot 10^{12}$, d) $3.5 \cdot 10^{12}$ $/\text{cm}^2$ n-type; $V_D=15\text{V}$.

Fig. 5. Transfer curves for different barrier implants at $V_D=5\text{V}$. Dotted line – FET, continuous line – SGT.

Fig. 6. Intrinsic gain as a function of drain voltage for different substrate doping levels; $V_{\text{SAT1}} \approx 1.5\text{V}$; $V_{\text{SAT2}} \approx 7\text{V}$.

Fig. 7. Intrinsic gain for a) $1 \cdot 10^{13}/\text{cm}^2$ P and b) $5 \cdot 10^{13}/\text{cm}^2$ BF_2 measured at $1\mu\text{A}$. $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d=10\mu\text{m}$, $0.5 \cdot 10^{12}/\text{cm}^2$ n-type bulk doping. Also shown is the gain of an equivalent FET.

Fig. 8. Computed variation of current and current density through the source as a function of source length. Current mismatch was calculated for a $0.1\mu\text{m}$ change in source length.

Fig. 9. Output characteristic for a high current, low barrier device at two operating temperatures, showing an increase in saturation voltage and low temperature coefficient.

$V_G = 0, 5, 10, 15$ V.

Fig. 10. Activation energy plot for the transistor in Fig. 9.

Fig. 11. Change of activation energy for current transport for a) a SGT having a high barrier and b) a SGT with a low barrier.