Effects of Process Variations on the Current in Schottky Barrier Source-Gated Transistors

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Abstract — The sensitivity of the drain current in Schottky Barrier Source-Gated Transistors to process variation is studied using computer simulations. It is shown that provided the device is designed correctly, the current is independent of source-drain separation and is insensitive to source length variations. However, uniform insulator thickness and precise control of the source barrier is needed if good current uniformity is to be obtained.

Index Terms — Source-gated transistor, thin-film transistor, polysilicon, Schottky barrier, process variations.

I. INTRODUCTION

In this work we evaluate the changes in drain current of Schottky Barrier Source-Gated Transistor (SBSGT) due to process variability. The Source-Gated Transistor (SGT) [1] has been demonstrated in polysilicon [2] and amorphous silicon [3] with a Schottky barrier contact between the source electrode and the semiconducting material. Figure 1 shows a schematic cross-section of the device.

From an electrical point of view, the SBSGT is formed of a reverse biased metal-semiconductor barrier at the source in series with a parasitic FET. The gate electrode completely overlaps the source barrier. Therefore, applying a voltage on the gate has the following simultaneous effects:

- Lowering the effective height of the source barrier
- Modulation of the conductivity of the parasitic field-effect transistor (FET) channel formed between the source and the drain;

Figure 2 depicts the band diagram between the source

and the gate.

Figure 1. Schematic showing cross-section of SBSGT

In this type of device, saturation occurs when the area under the source is depleted and the current that flows into the channel is restricted by the source barrier. As a consequence, the channel length of the parasitic FET is of little importance and the output characteristics of such a device are much better than those of a standard FET even at very small source-drain separations. The SBSGT is a good candidate for use in high performance large area electronic circuits due to the high output impedance and low saturation voltage [1].

Figure 2. Band diagram between the source and the gate of an SBSGT

This work assesses the tolerance to process variability of the drain current of the SBSGT with the aim of formulating suitable design rules for high performance large area integrated circuits containing SBSGTs.

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II. SIMULATION RESULTS AND DISCUSSION

A. Device structure and simulation environment

A standard SBSGT structure [1] has been investigated using the Silvaco Atlas 2D physical simulation environment.

Table I describes the symbols used. The semiconducting material is n-type polysilicon and the insulator is silicon oxide. For the default structure the drain contact is ohmic, there is a metal-semiconductor barrier at the source and the gate overlaps the source completely (see Figure 1).

TABLE I. GEOMETRICAL AND ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Default value
Source length	SL	$1\mu\text{m}$
Source-drain separation	d	$1\mu\text{m}$
Device width	W	$1\mu\text{m}$
Insulator layer thickness	tox	50nm
Semiconductor thickness	tsi	10nm
Schottky barrier height	Φ_B	0.35eV

B. Source length simulation

Simulations have shown [4] that the current transport over the potential barrier has the greatest magnitude at the edge of the source closest to the drain.

Figure 3. Variation of drain current with source length for three values of gate voltage

This feature is shown in Figure 3 where the source length (SL) is relative to the edge opposite the drain. It can be seen that there is a certain SL value above which the current is insensitive to process variations of SL. This value increases with gate bias and is attributed to the fact that the conductivity under the source is larger and there is a contribution from regions further from the source edge.

We conclude that the source should be kept as short

as possible in order to minimize the source-gate capacitance for optimum a.c. performance but above a specific value to maximise the current and use a regime where the output current is insensitive to process variations of SL.

C. Source-gate overlap simulation

This simulation is an extension of the one discussed in B. The source has a length of $1\mu\text{m}$ but the gate does not overlap the source completely. The results are plotted in Figure 4. For a large overlap, the simulation shows the same results as in Figure 3. The effective source length is in fact the length of the source-gate overlap.

The smallest overlap in Figure 4 corresponds to the case when the structure is a regular FET with a Schottky source barrier and no (or accidental) source-gate overlap. In this case the gate field does not act fully towards lowering the effective barrier height and the drain current is severely limited.

Even for zero overlap the current changes slightly with gate bias, indicating that there is some barrier lowering. This can be attributed to the fringe fields of the gate that act on the source even when the two do not overlap physically. The design recommendation is to design the transistor with a source-gate well within that required to maximize the current (e.g. 50% for $V_{GS}=6\text{V}$).

The process variation in source and gate patterning and their relative alignment should have minimal effect on drain current consistency from device to device, provided that the design criteria outlined in the previous subsection are met.

Figure 4. Variation of drain current with source-gate overlap for three values of gate voltage

D. Source-drain separation simulation

One of the main advantages of SGTs is the fact that

the drain current is independent of source-drain separation (d , equivalent to the length of the parasitic FET in series with the source barrier) [2], [5]. This means that the high output impedance in saturation and the low saturation voltage are maintained even when d is decreased to well below $1\mu\text{m}$.

Figure 5. Variation of drain current with source-drain separation (parasitic FET channel length) for three values of gate voltage

As can be observed from Figure 5, at high gate bias the drain current remains constant when d is varied from $2\mu\text{m}$ to $0.2\mu\text{m}$. For longer source-drain gaps, the current starts to decrease, more so for $V_{GS}=6\text{V}$ than for $V_{GS}=8\text{V}$. The reason for this drop can be attributed to the reduced conductance of the parasitic FET channel for longer d . This is confirmed by the $V_{GS}=4\text{V}$ plot.

Figure 6. Variation of drain current with insulator thickness for three values of gate voltage

From an integration point of view it helps to have smaller devices. Keeping d under $1\mu\text{m}$ also has some other advantages such as the possibility of operating at lower gate bias for high current output and high switching speed. In organic materials in which the effective carrier mobility is drain field dependent, a short source-drain gap leads to increased electrical field and faster device operation [6], [7].

Referring back to Figure 5, it can be concluded that

the on-current of the SBSGT is independent of d in saturation. The most important implication of this fact is that SGTs are well suited to be made with consistent performance with large-volume techniques (such as printing, stamping or lift-off) in which high accuracy cannot be achieved due to speed of manufacture and cost implications.

E. Insulator thickness simulation

The dependence of drain current on insulator thickness is shown in Figure 6.

It can be observed that even small changes in insulator thickness can have a significant effect on the on-current.

t_{ox} influences both the FET channel conductivity and the magnitude of the field that pulls down the source barrier. Since for this structure the on-current in saturation is limited by the source barrier (see subsections B. to D.), we can state that it is the latter effect that has the greatest contribution.

Good insulator uniformity across the wafer is desired and the usual matching techniques should be used during the circuit design stage.

Figure 7. Variation of drain current with semiconductor thickness for three values of gate voltage

F. Semiconductor thickness simulation

As with t_{ox} , the thickness of the semiconductor, t_{si} , has an impact on both the channel conductance and the barrier-lowering gate field. The behaviour of the SGT is also influenced by the relative ratios between the semiconductor layer capacitance and insulator capacitance [3].

In this particular structure it can be observed (Figure 7) that the change of drain current with semiconductor thickness is dependent on gate voltage. For this particular simulation this is a minimum at about $V_{GS}=4.8\text{V}$. The change increases as the gate voltage is raised above 4.8V and the current increases. Therefore for high current small variations of t_{si} may result in

unacceptable changes of the on-current.

The existence of a value of the gate bias for which the drain current dependence on t_{si} is minimal prompts the analytical investigation of this phenomenon. Establishing variability-aware design rules for any given t_{si} , t_{ox} and dielectric properties of these layers would help ensure optimum performance in large area, low-cost technologies.

G. Schottky barrier height simulation

In Figure 8 we show the dependence of on-current on the source barrier height. This type of plot is useful in visualizing the effect of having a source barrier in series with a finite conductance FET channel. For low barriers, the FET channel limits the current, whereas for high barriers, the barrier itself is the limit. The device is more FET-like at low gate bias, where the channel conductance is low and more SGT-like at high gate voltage.

Figure 8. Variation of drain current with Schottky barrier height for three values of gate voltage

In order to get significant on-current levels, a balance needs to be achieved between the two, but as the barrier gets lower and the device behaves more as an FET the high output impedance in saturation starts to suffer and saturation occurs at a higher drain voltage.

We see from Figure 8 that the drain current is very sensitive to the magnitude of the source barrier height. However, we require low barriers for high current operation and these are easier to control particularly in semiconductors that contain a lot of states. Furthermore, current transport across the barrier is thermally activated [8] and on-chip temperature variations can lead to significant changes of drain current. Circuit design techniques such as matching, differential signal processing, current driving and temperature compensation should be used. Special attention should be paid to the conditions (gate bias, supply voltage, t_{si} , t_{ox} , source metal) needed for maintaining the SGT-like

operation at high temperature where the barrier is lower.

III. CONCLUSION

We have performed an analysis of the drain current tolerance to process variability in the Schottky Barrier Source-Gated Transistor. The current is immune to source-drain separation (d) variations and insensitive to source length but good control of insulator thickness and Schottky barrier height is needed.

Current uniformity can be optimized further by choosing suitable biasing, adapted to the technology used.

Interestingly, if uniform frequency response is required rather than uniform drain current then it is found that variations in insulator and semiconductor thicknesses are not important [9].

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