Design of Power FETs Based on Coupled Electro-Thermal-Electromagnetic Modeling

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Abstract — A comprehensive modeling approach is applied to the study of pHEMT transistors for microwave power amplifier applications. This approach combines physical, electromagnetic and thermal simulations to model large power transistors used in these applications, allowing both the individual finger contribution and the global performance to be investigated in an efficient manner, which can be used with commercial CAD tools. In this way the design of the transistor structure contributes to the optimization of the RF performances of the complete amplifier. Discrete transistor and MMIC designs are investigated using this work with validation based on infra-red and microwave measurements.

Index Terms —Power transistor model, physical, electromagnetic and thermal simulations

I. INTRODUCTION

This paper describes the application of a combined model incorporating electromagnetic, physical and thermal simulations to analyze large pHEMT transistors (Fig. 1.). The model permits the investigation of the individual gate finger cell contributions to the output power as well as the temperature gradients present in these large devices (Fig. 2.). This allows the device to be optimised for particular applications and operating frequencies and has been found to be of particular significance for high power devices (up to 120 Watts at 2 GHz) and millimetre-wave power amplifier MMICs.

Fig. 1. Filtronic 96 mm power pHEMT.

The response of the entire device is predicted using electromagnetic and physical analysis. The procedure allows the investigation of the role of the geometrical dependencies, including the gate and drain feed networks and the internal operation of large multi finger devices to be investigated [1].

This modeling methodology is completed by a coupled thermal analysis of the transistor. FET devices are not subject to the critical thermal runaway experienced with HBTs, but the temperature sensitivity of the parameters is significant for all types of power transistors. The main effect of temperature increase is an output current reduction due to the lower electron

mobility, impacting gain, impedance match and power handling. Using the thermal simulation, the self-heating of each of the cells resulting from power dissipation as well as the thermal interaction between each cell is characterised. The thermal behaviour is included in the model using a thermal matrix scheme [7]. The scheme is really easy to expand to the studied power transistors with large numbers of fingers.

One of the objectives of this approach is to examine the high efficiency operation of the complete microwave amplifiers, such as class E and F designs, and derive the optimal design of the transistor and embedding circuit. This technique is being considered for designs in the frequency range 1 GHz to 38 GHz, with device peripheries of up to 220 mm.

Fig. 2. Thermal infra-red picture of a 60 mm power pHEMT, showing temperature variation across the die at $V_{DS} = 12V$ and $I_D = 2.7 A$ (Device courtesy of Filtronic plc).

II. DEVICE MODELING

A. Physical and Electromagnetic Simulations

The simulation of the device is conducted by considering two separate regions of the structure: the electrode metallization on top of the substrate and the regions inside the semiconductor located beneath the electrodes in the active epitaxial region.

The first region is simulated as a whole for the complete device using electromagnetic simulation based on the method of moments. The Momentum simulator has been used in this work. This enables all the distributed and coupling effects arising inside the transistor to be readily taken into account [2]. The simulation is not limited to the actual transistor but also includes its environment. The effects of surrounding via-holes and passive components are taken into account too. The usual extrinsic parasitic equivalent circuit can still be extracted from

Fig. 3. Detail of the modeling approach: (a) transistor layout, (b) association of one active cell model with the electromagnetic simulation, (c) intrinsic unitary cell model: the thermal dependence of the resistance matrix scheme takes into account both the self heating from the finger dissipation and the temperature increase resulting from the other fingers using a thermal matrix.

the electromagnetic simulation data if desired. The information provided gives the opportunity to rate and compare different metallization patterns easily from the point of view of performance and ease of realisation.

The second region, represented as a cross-section of the active region of the transistor, is simulated using a physical simulator: the Leeds Physical Model [3]. A hot electron quasi-two-dimensional transport description including thermal effects is used to self-consistently solve the Poisson, current continuity, energy conservation and two-dimensional Schrödinger equations for the device cross-section [4]. The device cross-section is described by the geometrical parameters (contact widths and spacings as well as recess depths and positions) and the epitaxial wafer structure including delta and bulk layers dopings. The simulation gives access to the DC characteristics with the S parameters, and is also valuable in characterising the non-linear behaviour of the active region when the device is operated in large signal mode (for example using time-domain simulation).

The physical simulation is done for each “unitary cell” (each source-gate-drain association) and then combined with the electromagnetic simulation. Each cell is subsequently represented by either a linear or non-linear equivalent circuit extracted from the physical simulation results, compatible with conventional CAD software. Each of the n “active” cells is connected to the corresponding source, gate and drain contacts of the electromagnetic structure, subsequently giving the response of the complete transistor in a way presented Fig. 3.

B. Thermal simulation

The thermal modeling is studied by solving the heat flow equation:

$$\nabla \kappa(T) \nabla T(x, y, z) = 0 \quad (1)$$

at the top of the substrate ($z=0$) using the methodology described in [5,6]. Thermal simulations are performed using HeatWave [7], a thermal analysis software written using a double Fourier expansion technique. For these simulations, the bottom of the substrate is attached to a heat sink with the temperature held at a constant level, and all other surfaces except

the heat sources are assumed for simplicity to be adiabatic (this has been shown to be a good approximation [7]). The total power of the distributed dissipating heat sources is determined by the product of operating DC voltages and currents flowing in the device.

The results from the physical simulation on Fig. 4. show that the maximum of the electric field is slightly shifted toward the drain contact at high voltages close to forward gate bias. This results in the power dissipation area (heat generation) being shifted in that direction too [8]. However, considering the small offset relative to the other dimensions, the locations of the heat sources are for convenience approximated to be the same as the gate fingers in the active region. The same set of data is then used for all simulations. It is also assumed that the heat dissipation is distributed uniformly over the surface of the gate fingers.

Fig. 4. Electric field distribution in one recessed area of the transistor.

The thermal simulation provides the temperature distribution at the surface of the substrate (Fig. 5.). The maximum temperature is extracted and compared for different gate widths and structures as in Fig. 6. The characteristic can be explained by considering the ratio of the passive area (contact pads, via holes, feed networks etc ...) to the “hot” area (transistor fingers) which decreases with the number of fingers. This results in a maximum temperature characteristic that is asymptotically uniform in very large devices for a given dissi-

pated power density (DC) and when all the cells operate with a uniform power dissipation. The figure also shows the well know benefit of substrate thickness reduction. The non-uniform power dissipation is considered later in this paper.

Fig. 5. Contour plot of surface temperature (°C) for a 10 finger FET (w=500 micron). The dissipated power is 0.3 W/mm.

Fig. 6. Maximum temperature in devices of different sizes for the same dissipated power density (0.3 W/mm).

III. DEVICE SIMULATION

The results of the preceding simulations are combined in the circuit simulator. The thermal results are included using a thermal resistance matrix scheme [7]. The same thermal analysis software is used to directly calculate the thermal resistance matrix. The temperature increases of each of the active cell are given by the equation :

$$[T - T_0] = R_{TH}[P] \quad (2)$$

with P the vector of power dissipation in each cell.

For a symmetrical device, only n/2 thermal simulations need to be run. The simulation process is further accelerated by restricting it only to the channel regions. The elements of the matrix are calculated using the averaged temperatures on these

regions. The calculated thermal resistance of the individual fingers for devices of different finger widths (total width is held constant) are presented Fig. 7. It appears that the improvement from substrate thinning is almost exclusively due to the reduction of the thermal coupling between fingers.

Fig. 7. Individual finger thermal resistances in devices with different number of fingers for the same **total** gate length and dissipated power.

The thermal results are included in the electrical model using a thermal command term and only taking into account the output current temperature dependency. Fig 8. presents the DC current of two cells located in the middle and at the border of the device. A much stronger effect of the temperature increase is seen where the device is hotter.

Fig. 8. Individual cell DC characteristics – $\circ$ centre, $\square$ periphery

The simulation of a larger power device (18x500 um) is presented in Fig. 9, using a Parker-Skellern large-signal CAD model [9]. The figure presents the contribution of each of the fingers to the output power. The simulation reveals a power peaking on external fingers. The counterpart thermal results are presented Fig. 10. This approach is also being applied to larger devices.

Fig. 9. Individual cell output powers at $f_0=2$ GHz, Class B with harmonic tuning.

Fig. 10. Individual cell temperature increases.

It has been observed both theoretically and experimentally that the temperature variation across the transistor is a function of harmonic matching (both at the input and output). Fig. 11. shows two different measured temperature distributions for a 96 mm power pHEMT operating at 50 Watts with differing load terminations.

Fig. 11. Temperature distributions of a power pHEMT supplying 50 W RF for two different harmonic matches.

These results show that the contribution to large-signal RF output power is not uniform across the device. Furthermore, the interaction between the electromagnetic, thermal and electronic properties of the device can lead to non-optimal performance when the FET is inserted into an amplifier circuit. Careful design of the device and circuit allows excellent performance to be obtained from power pHEMT devices, for example: 55 Watts CW, 59% PAE, 55 °C at 2.1 GHz (96 mm

width); 30 W CW 78% PAE, 32 °C at 870 MHz (48 mm width), with harmonic tuning. MMIC designs for Class E amplifiers, based on this design optimisation technique are currently in fabrication.

VII. CONCLUSION

An electromagnetic, electro-thermal microwave model for a pHEMT power transistor has been presented. This model allows the investigation of the electrical, RF, large-signal performances and the thermal properties of large power devices. This in turn allows the optimal design of power amplifier and power device based on optimisation of the device structure, device metallization layout and embedding circuit elements.

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