Source-Gated Transistors in Poly-Silicon

J. M. Shannon, D. Dovinos, F. Balon, C. Glasse, and S. D. Brotherton

Abstract—Source-gated transistors (SGTs) have been made in thin layers of polysilicon formed by excimer laser crystallization of amorphous silicon. It is shown that the main features of the SGT, namely a low saturation voltage and high output impedance can be obtained in poly-silicon. Furthermore the nature of the source barrier enabled it to be pulled down by the influence of the gate to low values giving small activation energies for current transport and reduced temperature sensitivity in the on-state.

Index Terms—Poly-silicon (poly-Si), Schottky barriers, semiconductor devices, thin-film transistors (TFTs).

I. INTRODUCTION

SOURCE-GATED TRANSISTORS (SGTs) [1] form a class of transistors in which the current is determined by the magnitude of the electric field at a reverse biased source barrier. This electric field is controlled using a gate located above or below the barrier. To date, source-gated transistors have only been made in hydrogenated amorphous silicon (a-Si:H) [2] where it has been shown that they can have a low saturation voltage, high output impedance and very much better stability than an equivalent field-effect transistor (FET) [3]. These features in a-Si:H makes the SGT well suited to OLED and PLED pixel drivers and small signal analog amplifiers [4].

With reference to Fig. 1, electrons will accumulate at the semiconductor-insulator interface when a large positive voltage is applied to gate relative to the source. However when a positive voltage is applied to the drain the source barrier is reverse biased and source-drain current is determined by electron transport across the reverse biased source barrier and its field dependence. Current saturation with drain voltage occurs when the semiconductor layer under the source barrier is depleted by the reverse biased source barrier. Since this layer is thin and lightly doped, saturation voltages are small. When saturation occurs it is a good approximation to assume that the gate insulator and semiconductor layer behave as two dielectric in series. This dielectric model enables the change in saturation voltage with the gate voltage to be calculated in a straightforward manner [2]. For drain voltages above saturation the electric field at the source barrier is determined by the magnitude of the gate voltage. Therefore we have a situation where the on-current of the device is determined by the reverse biased source

Fig. 1. Schematic cross section of bottom-gate SGT in poly-silicon.

barrier, while the off-current is determined by the parasitic FET of length d in series with it.

The output impedance of a SGT can be very high because the source barrier is screened from the drain field by the gate located directly opposite to it [1]. This is in contrast to a FET where an ohmic source region is exposed to the drain field emanating from the laterally spaced drain contact. The SGT is therefore much more tolerant to deleterious short channel effects [5].

Here we are concerned with the SGT in polysilicon (poly-Si) where the very low saturation voltage at high gate voltages and high output impedance of the SGT compared with FET should provide attractive benefits for a variety of circuit functions. It is shown that indeed these features are found in a poly-Si SGT.

II. SAMPLE PREPARATION

SGTs in polysilicon were made by adapting a mask set used for making standard FETs and using a technology based on excimer laser crystallization of amorphous silicon. Both top and bottom gate structures have been made in the past using and excimer laser [6]–[9] but we chose a bottom gate structure because the source barrier was then on the surface and easily accessible for barrier modification studies. A top gate structure could be used but the source barrier would need to be under the polysilicon and therefore has less flexibility in respect to barrier control. A schematic cross section of the SGT structure is shown in Fig. 1. This structure was far from ideal particularly the gate-drain overlap but enabled us to check the basic properties of a SGT. The bottom gate structure was made using an excimer laser to crystallize an amorphous silicon layer deposited on top of the oxide by plasma-enhanced chemical vapor deposition [10]. The thicknesses of the oxide layer and poly-Si layer were 150 and 40 nm respectively. A field-plate structure to provide field relief at the edge of the Schottky source barrier was made by depositing a thin oxide (43 nm thick) on the top of the poly-Si and overlapping the source contact metal to form the field plate. A Schottky source barrier was formed using chromium backed

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Fig. 2. Output characteristics of polysilicon SGT, $d = 10 \mu\text{m}$.

Fig. 3. Transfer characteristics corresponding with the SGT shown in Fig. 2.

up by aluminum. The n^+ drain region was formed using phosphorus ion implantation through the field plate oxide with the source metal acting as a mask. The source/barrier gate overlap was nominally fixed at $3 \mu\text{m}$ but the channel length d of the parasitic FET varied between 2 and $60 \mu\text{m}$. The width w of all the devices was $50 \mu\text{m}$.

III. RESULTS AND DISCUSSION

The output characteristics of a poly-Si SGT with a Schottky source barrier is shown in Fig. 2 along with the corresponding transfer curve in Fig. 3. The characteristics have the main features of a SGT, namely a low saturation voltage and high output impedance. The characteristics of bottom-gated FET structures with ohmic source regions showed much lower output impedances and the saturation voltage changed by approximately 1 V for every additional volt on the gate and were similar to these found in top-gated structures [11]. Furthermore the saturation current of the SGT at a given gate voltage was independent of d , the length of the channel of the parasitic FET (Fig. 4) which shows that the current is controlled by the gated source Schottky barrier and the transistor is operating as a SGT. The magnitude of the current depends on the effective barrier height of the source barrier.

Fig. 4. Saturated drain current at $V_g = 10 \text{ V}$ through a SGT against source/drain separation (d). The activation energy of the transport process was obtained from the slope of $\log I_d$ versus $1/kT$.

It is seen in Fig. 2 that the impedance is high at low drain voltages but it is compromised by the poor performance of the field-plate passivation structure and the current increases markedly above $V_D = 6 \text{ V}$. At low drain voltages impedances exceed $10^9 \Omega$.

Typical of SGTs, the saturation voltage is low. With $V_G = 12 \text{ V}$, for example, $V_{\text{SAT}} < 2 \text{ V}$ which compares with $\sim 9 \text{ V}$ for a FET ($V_G - V_T$). At higher gate voltages V_{SAT} increases by $\sim 0.12 \text{ V}$ for every volt on the gate which is higher than the 0.08 V per 1 V on the gate we expect from the dielectric model for the SGT [2]. This could be due to states at the poly-Si oxide interface. The slow increase in current with the gate voltage in the subthreshold region of the transfer curve (Fig. 3) also suggests that there are large number of interface states which is not surprising in a laser crystallized bottom gate structure.

The activation energy E_A for current transport in the off-state ($V_G = 0 \text{ V}$) and on-state ($V_G = 12 \text{ V}$) is shown in Fig. 4. Since the off-state is controlled by the parasitic FET the value of 0.52 eV is roughly what we would expect since this value is close to half the band gap of the silicon and consistent with a generation current. In the on-state however when the current is determined by the reverse-biased Schottky barrier the activation energy is very much smaller than expected based on thermionic-field emission of electrons through the barrier. Using the known tunneling constant for silicon [12] the effective barrier height and the activation energy should change by $\sim 0.01 \text{ eV}$ per volt on the gate but we have measured values five times higher than this. A possible explanation is that there is an insulating interfacial layer between the Cr metal and the polysilicon resulting in a significant contribution to the current from field emission of carriers rather than purely thermionic-field emission. The presence of an insulating layer would also explain why the current is very much lower at $V_G = 12 \text{ V}$ than we expect from a barrier with an effective barrier height of only 0.17 eV . If the insulating layer was SiO_2 then it would need to be $\sim 2 \text{ nm}$ thick to account for the large change in the barrier height.

The low activation energy in the on-state has important implications because the change of current with temperature is small

and the transistor is nearer to the ideal zero temperature coefficient. In fact we have measured E_A in some transistors as low as 0.08 eV at $V_G = 12$ V.

The SGT is well suited to circuits where lower power dissipation is required because it can be operated in saturation at low drain voltages. Of course a FET can also be operated in saturation at low drain voltages provided the gate voltage is not much greater than the threshold voltage. However it is in this region of the FET that the current is most sensitive to small changes in threshold voltage. In contrast, the SGT can be operated at high gate voltages well away from the threshold where the effects of threshold variations and instability are negligible, particularly since device stability is sensitive to drain field rather than gate field [11].

IV. CONCLUSION

SGTs have been formed in polysilicon made using excimer laser crystallization. SGT behavior in these thin film transistor structures with a Schottky source barrier was verified by the fact that the drain current was independent of the channel length of the parasitic FET. The magnitude of the drain current was therefore defined by the effective height of the source barrier and its dependence on the electric field induced by the gate.

The output characteristics showed the main features of a SGT, namely a low saturation voltage and high output impedance. The output impedance at high drain voltage, however, was severely degraded by the failure of a field-relief passivation region at the edge of the Schottky source barrier.

Activation energy measurements in the on-state showed much lower values than expected. The low values could be accounted for by the presence of a thin insulating region at the interface between the Schottky metal and the poly-silicon. An important

advantage of low activation energies is that of a low temperature coefficient for the on-current.

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