Down-scaling of Thin-Film Transistors: Opportunities and Design Challenges

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With the ever-increasing demands for integration of advanced electronic functions into large-area electronics, down-scaling of thin-film transistors (TFTs) becomes very necessary. The key device operational issues associated with TFT scaling, including short-channel effects (SCEs) and self-heating, are considered in this paper. Device structure engineering approaches are introduced to suppress the SCEs for designing short-channel TFTs with excellent digital and analog performance. And electro-thermal simulation results show that the self-heating in TFTs will be much more significant than that in silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) due to the substrate of poor thermal conductivity. Enhancing the heat dissipation by placement of metal heat pipes in the cap dielectric layers is proved to be an effective way to deal with the heating issues.

Introduction

Thin-film transistors (TFTs) have the similar structures and operation principles with the crystalline silicon (c-Si) metal-oxide-semiconductor field-effect transistors (MOSFETs), but are constructed on inexpensive substrates of low thermal budgets such as glass and plastics for large area electronics. Although the development of TFT technologies in the past is mainly cost-driven to maintain compatibility with low-cost large-area manufacturing, performance improvement of TFTs is demanded more and more due to the rapid revolution in electronics design. The applications of TFTs have gone far beyond the conventional role as pixel switching in active-matrix displays, and require higher speed, lower operation voltage and increased integration density to meet the design requirements, for examples of the following three aspects: 1) At a display pixel level, advanced devices and circuits need to be integrated to correct for variations, compensate for device aging (1), and include storage or sensing functionalities for value-added displays (2), which however, are limited by the pixel area; 2) At a system level, integrating external driver ICs directly onto the same substrate will be able to relax the connection limits of pitch sizes for high-resolution displays, shorten the display manufacturing and inspection processes, and makes the assembly more robust and reliable (3); 3) There is growing interest world-widely to achieve advanced electronic functions for signal communication, processing and data storage on glass, plastic or fabrics substrates, which will enable a low-cost and flexible design solution to usher the age of pervasive electronics (4).

However, the quality of semiconductors is severely constrained by materials and substrate process limitations and result in TFTs of poor performance that needs high operation voltage and supports only low-frequency circuits. Although a number of venues have been explored for improving the quality of semiconductors growing on glass and plastics, including various forms of silicon (5-7), semiconducting organic materials (8),

oxide semiconductors (9) and some nanostructure films (10), there are no methods available yet to achieve TFT channel materials with mobility as high as c-Si for practical applications. Therefore, compared to c-Si MOSFETs, down-scaling of the channel length is even more demanded to achieve similar level of performance for TFTs.

To make short channel TFTs, achieving the required pitch resolution with well-controlled process in large area low-cost manufacturing is first of all a limiting factor. Now submicron technologies for silicon TFTs are available (11), and lots of research are on-going for low-cost pattern techniques for self-aligned gate sub-micron organic TFTs (12, 13). Compensation for process induced distortions is also critical to make TFTs on plastic substrates. This paper will focus on two device operational problems - short-channel effects (SCEs) and thermal issues in the small size TFTs, and discuss possible solutions.

Device Structures to Suppress Short-Channel Effects

To achieve high-speed TFTs, the most straightforward way is by shrinking the distance between source and drain to enhance the lateral electrical field and shorten the carrier transit time in the channel. But as a result, the influence of the drain on the channel also competes more and more with that of the gate, leading to the occurring of SCEs with an increased leakage current, degraded subthreshold swing and a reduced output resistance. For shorter channel c-Si MOSFETs, making thinner gate dielectric layer is important to maintain the strong electrostatic control of the channel from the gate, and various junction and doping technologies such as ultra-shallow junctions, halo implantation and lightly doped source/drain are also introduced to provide SCE suppression (14). Contrarily, for TFTs, it is very difficult to process high quality and very thin dielectric layer efficiently with high yield over large areas, and complicated junction and doping technologies are also not applicable. Two structure engineering methods are discussed here to overcome these obstacles:

Ultra-thin channel (UTC) structure

The structure configuration of TFTs is very close to that of silicon-on-insulator (SOI) MOSFETs. In a SOI MOSFET structure, as shown in the inset of Fig. 1, for suppression of SCEs to obtain good subthreshold characteristics, the structure parameters should generally meet the following relationship [15]:

$$L \geq A \sqrt{\frac{\epsilon_{ch}}{\epsilon_I} t_{ch} t_I} \quad [1]$$

where t_{ch} is the channel thickness, t_I is the gate-insulator thickness, ϵ_{ch} and ϵ_I are their permittivities, respectively. A is a factor, which ranges from 5-10, depending on the doping profile and the specific applications (low power or high performance). According to the relationship, making a thinner channel is also effective to suppress the SCEs. Drain-induced-barrier-lowering (DIBL) is a vital parameter to evaluate the SCEs. Fig. 1 shows the simulated DIBL versus L/t_{ch} across a large number of SOI MOSFETs with different channel length and channel thickness. It can be seen the DIBL is sufficiently sustained when L/t_{ch} is larger than 10. An ultra-thin channel can also reduce the sub-surface leakage or bulk conductivity of the channels, which dominates the off-state leakage in the TFTs made without junction technologies.

Figure 1. The simulation results of DIBL versus the ratio of the channel length to the channel thickness (L/t_{ch}) obtained by numerical device simulator Silvaco-Atlas. The simulated DIBL across a large number of devices with different channel length (L) and channel thickness (t_{ch}). A 10 nm thick silicon oxide is fixed as the gate dielectric layer.

Figure 2. Plot of the extracted threshold voltage (V_{th}) values for the 2.0 nm thick channel nc-Si TFTs in 100 different dies on a same chip, showing very good uniformity. Inset: cross-sectional scanning electron microscopy and transmission electron microscopy micrographs of the fabricated ultra-thin channel (UTC) nc-Si TFTs (the minimum channel thickness is 2.0 nm). The channel length is 0.5 μm , with the gate insulator of 22.5 nm effective oxide thickness.

When the channel film becomes thinner and thinner, there will be increased difficulties in terms of both device fabrication and understanding the electronic transport properties. For example, in very-thin small grain non-crystalline Si films, the random thickness variations may result in highly random potential due to a strong vertical quantum-confinement effect (QCE). Charge traps at grain-boundaries (GBs) and the oxide/Si interface will deplete the Si layer of free carriers, making the film resistivity

extremely high. In this work, nano-scale thin nanocrystalline Si (nc-Si) films were successfully deposited with precise control over the film thickness by chemical vapour deposition (CVD). TFTs made of these films, ranging from 8.0 to 2.0 nm in thickness, can thus function as normal MOSFETs (16). As shown in Fig. 2, the devices have very good intra-chip uniformity of electrical characteristics, even when the channel thickness is as small as 2.0 nm (16). Based on the simulation results in Fig. 1, the UTC structure is expected to be able to achieve deep-sub-micron or even sub-100-nm TFTs with good control of SCEs.

For disordered silicon transistors, the performance is compromised by an anomalously high leakage current due to defect states that are present in the bandgap, which is exponentially dependent on the bandgap of the material (E_g) (17). When the transistor channel becomes shorter, the influence of the drain on the channel grows, resulting in an increased subthreshold leakage current when the gate voltage is below the threshold voltage. This subthreshold leakage is also exponentially dependent on E_g . When the silicon film thickness is reduced to a few nanometers, QCE results in the modulation of the band structure, which gives rise to band edge shifts in both the conduction and valence bands relative to bulk silicon, thereby effectively increases E_g (18). Directly attributable to this widened bandgap, the OFF-state leakage current (I_{OFF}) decreases significantly in the ultrathin channel transistors, as shown in Fig. 3(a), whereas bandgap widening has a much less pronounced effect on the ON-state current (I_{ON}). The gate voltage required to switch the transistor between ON and OFF states also decreases because of a stronger gate control of the channel surface potential in thinner channel transistors (19). These result in a higher I_{ON}/I_{OFF} ratio, which exceeds 10^{11} for devices with a 2.0-nm-thick channel, as shown in Fig. 3(b). The high I_{ON}/I_{OFF} ratio will allow for applications where low power and fast access times are demanded and crucial (20).

Figure 3. (a) The leakage-current (I_{OFF}) as a function of nc-Si channel thickness (t_{Si}) (■: experimental results; —: theoretical calculations). Inset: the subthreshold swing (S) as a function of t_{Si} (○: experimental results; —: theoretical calculations); (b) The I_{ON}/I_{OFF} current ratio as a function of nc-Si channel thickness (t_{Si}).

Source-gated transistor (SGT) structure:

For analog operation, good gain requires a high transistor output resistance, which is to say, the transistor current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the sensitivity of the transistor current to the drain voltage is increased. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers (21).

Figure 4. Schematic of a source-gate transistor (SGT)

The SGT structure is proposed to realize good analog performance while the TFTs are scaled down (22). In the SGT structure (Fig.4), there is a potential barrier formed at the source contact. The gate lies under the source barrier and extends across to the drain contact. When the transistor is switched on, the barrier controls the on-state current and saturation is governed by the electrostatics at the source barrier. Here the “pinch-off” is at the source edge rather than the drain end of a channel in the traditional FETs, as shown in Fig. 5. The geometry of the SGT leads to much less susceptibility to SCEs and a higher output resistance due to the source barrier being screened from the drain field by the gate.

Figure 5. Numerical device simulations by Silvaco-Atlas showing 2D distribution of carrier concentration in the SGT for different drain voltages (a) 0.1V, (b) 2.5V, (c) 15V and $V_G=10V$. The thickness of the semiconductor (a-Si:H) and the insulator (SiN) is 100nm and 300nm respectively.

The intrinsic voltage gain g_m/g_d has been measured for both a SGT and a FET made using the same layers of gate insulator (300nm SiN) and a-Si semiconductor (100nm). Although the g_m of the FET was higher than of the SGT it had a much lower voltage gain because of the poorer output impedance (23).

Figure 6. Measurements of the intrinsic voltage gain g_m/g_d for a SGT and a FET made using the same layers of gate insulator (300nm SiN) and a-Si semiconductor (100nm).

The SGT structure is also applicable to organic semiconductors (24). The simulated I_{SD} – V_{DS} characteristics of an organic SGT (OSGT) are compared to that of an organic FET (OFET) in Fig. 7 (25). Even with a 50-nm-thick SiO₂ layer, the submicrometer OSGT can be operated with extremely good output characteristic (Fig. 7(a)). In a comparison, the channel length (L) of an organic FET (OFET) must be extended to 5 μm to get saturated output characteristics, as shown in Fig. 7(b).

Figure 7. (a) Simulated output characteristics of the OSGT shown in Fig. 4 with a source–drain separation (d) of 0.5 μm , source length (s) of 1 μm , channel thickness of 30 nm, and SiO₂ layer thickness of 50 nm. (b) Simulated output characteristics of the OFET in the inset with the same layer thickness as that of the OSGT and channel length (L) of 5 μm . The gate to source voltage (V_{GS}) ranges as: 0, –1 V, . . . , –5 V.

Compared with the FET, the SGT is operated with much less excess carrier concentration, combined with much higher internal fields over small dimensions. The low carrier concentration improves stability, whereas high internal fields increase the

carrier velocity, provided the carrier velocity is proportional to the electric field (26). In many organic semiconductors, the mobility is field dependent. In material systems with disorder, to improve transistor speed very short channels are required to produce high internal electric fields (26). In the case for the traditional FET, achieving thin gate insulator layers of high quality to suppress the SCEs will be difficult, whereas the SGT can operate with very short source drain separations even with a thick gate insulator layer, thus providing a big advantage in terms of the fabrication process. Simulation studies suggest increased carrier velocity in organic materials for high drive current and frequency response that can be orders of magnitude higher than an FET (24). The current through an SGT is insensitive to source-drain separation, thus enabling current uniformity with simple and imprecise pattern techniques (24). Also high-speed and stable digital logic can be designed based on the devices by using the current-mode logic style (25).

Thermal Issues and Design Solutions

Figure 8. Schematics illustrating the heat flow in different technologies: (a) bulk MOSFET; (b) SOI MOSFET; and (c) TFT.

As the device geometries diminish as well as current density increase with the technology scaling, power densities will increase and make localized heat generation more and more pronounced. As shown in Fig. 8, in conventional bulk or SOI MOSFET IC chips, a majority of the heat generated in the channel conducts through the silicon substrate, then package and heat-sink. However, for TFT circuits and systems on a glass or plastic substrate, the substrate with extremely low thermal conductivity (e.g. 1.35 W/m.K in glass compare to 148 W/m.K in silicon) eliminates the thermal paths. Heat generated in the devices during operation cannot be efficiently dissipated via the interlayer oxide and substrate. Therefore, much more substantial self-heating effects are expected than that in MOSFET technologies. The heating induced local temperature increase will impair the device and circuit operation and cause reduced reliability and shorter lifetimes.

Figure 9. The simulated temperature contour in (a) the SOI MOSFET and (b) the TFT at $V_{GS}=4.0$ V and $V_{DS}=1.2$ V, showing a much higher temperature in the TFT channel due to self-heating. The temperature at the bottom and top of the simulation domain is fixed at the surrounding temperature of 300 K, on the assumption of idealized cooling. The left and right boundaries are set as thermal insulation.

Figure 10. Simulation data showing small-signal output conductance as a function of drain current for the TFT, and SOI MOSFET with and without considering self-heating. Output conductance was simulated at dc bias conditions, corresponding to the strongest dynamic self-heating effect.

To gain a deeper insight into electro-thermal effects in TFTs, the device characteristics of a $0.25\ \mu\text{m}$ gate length TFT on glass substrate is compared to a SOI MOSFET of the similar structure by Silvaco-Atlas numerical simulations. The TFT is assumed to have the same material properties with the SOI transistor only with a glass substrate instead of the silicon substrate, for comparison purposes.

Fig. 9 shows the temperature contours in the two devices at $V_{GS} = 4.0$ V and $V_{DS} = 1.2$ V. A much higher channel temperature can be observed in the TFT device than that in the SOI transistor. In the SOI MOSFET, the main thermal path is going through the thin

buried oxide layer and then the silicon substrate, which has good thermal conductivity. However, in the TFT device, heat generated in the channel during operation cannot be efficiently dissipated via the thick glass substrate which has poor thermal conductivity. Fig. 10 plots the output conductance, simulated at static conditions, as a function of drain current under $V_{DS} = 1.2$ V for the TFT and SOI MOSFET with and without turning on self-heating. The self-heating induces carrier mobility degradation and thus a reduction of drain current observed as a negative differential drain conductance. At the same gate and drain bias, the TFT has a much higher reduction of drain saturation current and stronger negative output conductance effect, compared with that of the SOI MOSFET. The results also indicate a higher device operating temperature and stronger self-heating effects in TFTs. Negative effect due to dynamic self-heating is more pronounced at lower frequencies, therefore the DC output conductance simulation represents the worst-case for dynamic self-heating (27). Negative output conductance is observed for the TFT device when the drain current reaches 0.45 mA, while, in the case of the SOI MOSFET, it does not occur until the drain current reaches 0.89 mA, clearly indicating a much more significant dynamic self-heating effect in the TFT.

The pronounced electro-thermal effects can be a vital consideration for analog circuit designs based on TFT devices. For instance, in the analog circuit design that employs current scaling of transistors for current sources, the difference in transistor dimensions, layout design, and the biased voltages will cause temperature spatial variations due to self-heating effects, and as a result the scaling factors will vary from the original values, which might significantly affect circuit characteristics (28). The self-heating induced degradation of drain current and AC small signal parameters may also seriously affect other key design specifications of the circuit including gain, bandwidth, etc. (29).

For the TFT, due to the thick substrate of poor thermal conductivity, the generated heat in the device channel has to be mainly dissipated through the oxide cap layer. The interconnect wires and vias above the device may help the heat dissipation. However, due to the high current density in these wires and vias for signal and power transmission, their effects on enhancing the heat dissipation might be exacerbated. To further improve the thermal performance, the effective thermal conductivity of the oxide cap layer can be improved through the fabrication of vertical metal heat pipes. These heat pipes do not necessarily transmit useful information and merely represent additional thermal paths to enhance the heat dissipation.

The analysis of a high-level system based on TFTs on glass is conducted by the solutions of the heat flow equations using the 3-D finite-element method (FEM). The simulated system structure is shown in Fig. 11 (a). The length and width are both 2 mm, and the system is composed of 18 circuit blocks. The constant temperature of 300 K is applied at both the bottom and at the top of the structure for perfect cooling, while the four side walls are set as adiabatic boundary conditions. Fig. 11(b) gives the power density for each function block in the IC with the average power density of about 60 W/cm². The simulated spatial junction temperature profile (extracted as the temperature at the surface of the active layer) of the system is shown in Fig. 12 (a). Significant temperature spatial variations can be seen, and the hottest region reaches 363 K. Localized metal heat pipe placement is used to remove the hot spot region at highlighted and reduce the temperature spatial variations, as shown in Fig.12 (b). The results indicate that during design stage, the placement of heat pipes can be optimized based on the spatial temperature profile obtained from primary simulations to remove the hot spots for better thermal performance as well as lower cost and higher electrical performance.

Figure 11. (a) The 3-D structure and related structure data for the FEM thermal simulations; (b) Functional circuit block layout showing power density associated with each block. The average power density is about 60 W/cm².

Figure 12. Simulated spatial junction temperature profile of the system (a) before placing heat pipes; (b) after placing 0.5% density copper heat pipes in the hot spot regions as highlighted, which occupies about 12.5% of the whole area.

Conclusions

The rapid revolution in electronics design provides more opportunities and demands for performance improvement of TFTs and thus downscaling of TFTs becomes more and more critical. Two challenges for continuous scaling of TFTs are discussed in details:

1) Device structures to suppress short-channel effects (SCEs)

As the transistor is scaled down, the resulted SCEs can cause increased leakage current and reduced output impedance. To suppress the SCEs, the first proposed structure is the ultra-thin channel transistor, in which, the strong quantum confinement induces a marked reduction of leakage current, and the subthreshold swing is also decreased due to strong electrostatic control of the channel from the gate, resulting in greatly improved switching performance. Another structure to be discussed here is the source-gated transistor. This structure uses gate modulated source barrier to control the current conduction and current saturation is determined by the electrostatics at the source barrier rather than pinch-off at the drain end of a channel, which leads to a much smaller susceptibility to SCEs and a higher output impedance because the source barrier is screened from the drain field.

2) Thermal-aware design

With the scaling of TFTs, the increase of power densities will make self-heating more and more pronounced. For TFT integration on glass or plastic substrates, the poor thermal conductivity of the substrate results in very high thermal resistance and thus much more serious self-heating effects are predicted than that in c-Si MOSFET technologies. The study shows that the metal wiring in the dielectric layers may help the heat dissipation in TFT based circuits and systems, and to further improve the thermal performance, dummy heat pipes can be fabricated in the dielectric materials as additional heat dissipation paths. The work also proposes a simple method to manage spatial thermal gradients and remove hot spots in high-level design.

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