Characterization and Modeling of LDMOS Power FETs for RF Power Amplifier Applications

(Invited Paper)

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Abstract—In this review we present a measurement-based approach to the creation of a successful circuit model of a high-power RF FET. We describe some of the measurement challenges that we face in the characterization and validation of the FET model, and our approach to their solution. We also outline some of the simulation and modeling techniques that are used in the construction of the complete transistor model. The model itself is fully nonlinear, with a self-consistent dynamic electro-thermal component, and includes the in-package matching and package components, which are derived from electro-magnetic simulations.

I. INTRODUCTION

The demand for accurate transistor models for RF and microwave circuit design has increased in recent years, as a result of the more stringent requirements that are placed upon power amplifier and transmitter designs by customers and regulating agencies.

Modern power amplifiers for wireless communications systems are tightly specified in terms of their linearity performance, bandwidth, etc., while at the same time the customers are requiring higher efficiency operation, realized by inherently nonlinear modes of amplifier operation such as Doherty, Envelope Tracking (ET), Class D and E switching amplifier modes, Class F harmonic tuning, and so on. The successful design of such RF power amplifiers can only be achieved through the use of CAD techniques, placing a premium on the availability of accurate nonlinear models for the transistor.

The combination of high powers and high frequencies in RF and microwave power amplifiers brings together a unique set of challenges for the device modeling engineer. The power transistors themselves are physically large, and may occupy a significant fraction of a wavelength, even at microwave frequencies. The electrical behavior in this distributed environment must be captured in the model. The device will generate a lot of heat, which must be dissipated effectively in the package. The thermal effects on the transistor's electrical behavior will also need to be characterized and modeled accurately.

Laterally-diffused MOS (LDMOS) FETs are used almost exclusively for high-power transistors for wireless infrastructure or base-station applications. They provide an unmatched combination of power and cost. In Fig. 1 we show a typical high-power transistor product, capable of delivering hundreds of watts of RF power. The complexity of the transistor in

Fig. 1. A high power LDMOS transistor with the package lid removed to show the complexity of the internal matching networks. This transistor is capable of delivering 140 Watts of RF power at 1 dB compression, at 2.1 GHz [1]. © 2006 IEEE. Reprinted with permission.

terms of the number of components is evident. Several issues need to be addressed in the construction of the circuit model of the product. For example, there will be electromagnetic interactions between the matching networks, bond-wires, etc. that need to be accommodated.

In this paper we shall outline an approach to the generation of a compact model of the power transistor that can be used in a circuit simulator for the design of RF power amplifiers. The model is derived directly from electrical and thermal measurements of the transistor, and so careful characterization is required. This presents a number of practical challenges in the measurements. The model construction preserves the dynamics and nonlinearities of the device, and so the model is considered to be an accurate representation of the transistor's behavior. A segmentation approach is used to build models for the active and passive components of the power transistor. This approach requires the careful definition of measurement and simulation reference planes, so that the component models can be constructed individually, and combined together with confidence. The model of the product can then be validated

against measured data that is taken in a different measurement environment from the characterization. We shall present some illustrative validation data.

II. THE SEGMENTATION APPROACH

In the design and modeling of a microwave packaged power transistor, linear models of the package and matching networks are combined with the nonlinear electrothermal model of the transistor. Our approach is to segment the transistor into its linear, nonlinear and thermal components systematically such that they can be recombined in a self-consistent manner.

The number of issues that must be addressed in a successful realization of a model include the electromagnetic (EM) interactions between the elements of the matching networks, and between the bond-wire arrays in the package; thermal management; the self-consistent integration of the thermal model with the electrical model of the device; and the construction of the nonlinear model of the transistor itself.

A. Electromagnetic simulation of passive components

The passive components surrounding the LDMOS die provide the necessary low-loss impedance transformation essential for the successful operation of the RF power amplifier. The matching networks are often composed of arrays of small-diameter bondwires, metal oxide semiconductor (MOS) capacitors, and packages, as illustrated in Fig. 1, or in the case of high-power RFICs, integrated spiral inductors, capacitors and transmission line elements.

Matching networks may contain several hundred bondwires all constrained in close proximity to one another within the package. Through the development of segmentation procedures, it is possible to divide the entire packaged transistor into portions, and simulate the components in finite-element and method-of-moments based simulators. The results are then appropriately combined, using network theory, to generate the model of the matching networks.

The separation procedure must not perturb the behavior of the components, i.e., the component when analyzed by itself must operate the same as it does within the larger device. This is ensured by careful calibration of both the measurement system and the simulation, to produce well-defined and accessible reference planes. The second issue is that any inter-element coupling, such as mutual inductance between arrays of bonding wires, must be properly characterized [1].

The results of applying these segmentation and simulation techniques to a large packaged device structure, similar to Fig. 1 except that the LDMOS die have been replaced by ground pads, is shown in Fig. 2, for the input return loss. The agreement between measures and modeled S-parameters is excellent, validating this modeling approach.

III. FET CHARACTERIZATION MEASUREMENTS

A small-signal FET model can be derived from S-parameter data, via Y-parameters. A typical equivalent circuit model is shown in Fig. 3, and the component values can be found from well-known expressions [2]. Such a model can be

Fig. 2. The magnitude of the simulated and measured input reflection coefficient of the device for the matching network when it is terminated in a short-circuit [1]. © 2006 IEEE. Reprinted with permission.

Fig. 3. Small-signal equivalent circuit model of the intrinsic transistor; this model is derived from Y-parameter measurements, with some admittance-to-impedance transformation in the GS and GD branches.

extracted as a function of the applied gate and drain bias, yielding a Bias-Dependent Linear FET model that can be used in small-signal AC or S-parameter simulations. The bias-dependent S-parameter measurements can be made using a vector network analyzer, and voltage supplies and current meters, or general-purpose stimulus-measure units (SMUs) controlled by commercially-available tools such as Agilent-EEsof IC-CAP™. This approach works well for small transistors, where the currents are low and the self-heating of the device is minimal. Often, such measurements are performed on-wafer, where the thermal environment can be controlled using a temperature-controlled chuck.

Power transistors are usually quite large in terms of total gate periphery, and this presents a number of problems in measurement. First, the currents drawn can be quite high, leading to unacceptable self-heating in DC measurements the device dissipates a lot of heat, and the channel temperature is not uniform over bias, leading to an ill-defined model. Further, the large periphery means that the gate and drain impedances that the device presents at RF can also be very low. This can cause oscillation in a 50 Ω measurement system. The problems of high current demand and potential

for oscillation generally place an upper limit on the transistor size for model characterization measurements. Even so, using transistors of up to 5 mm total gate periphery are not uncommon for power transistor characterization.

Pulsed techniques are frequently used for the I-V and S-parameter measurements for characterization of power transistors for model extraction. Pulsed measurements offer a number of advantages over DC measurements. The energy input to the device is determined by the pulse width and the duty cycle, enabling the temperature of the transistor to be controlled, yielding isothermal conditions over the whole measurement set. The use of short time pulses enables us to measure in regions of the output I-V characteristics that would otherwise be inaccessible under DC conditions, because of thermal power dissipation limits, or voltage breakdown limits. This enables us to produce a model that can predict the device operation more accurately under real drive conditions, where the instantaneous or RF load-line trajectory lies beyond the DC limiting conditions. Further, by varying the pulse width and measurement times, we can identify trapping phenomena in the transistor. This is mainly of interest for III-V devices: LDMOS does not suffer from long time constant trapping phenomena.

Pulsed measurement also have some limitations. In particular, the dynamic range of RF S-parameter measurements can be significantly degraded, limiting the measurement accuracy. This is also a result of having low energy in the sampled pulse. The use of averaging can improve the signal-to-noise ratio, at the expense of measurement time. Recently-introduced pulse measurement instrumentation can overcome such dynamic range problems by careful signal processing of the received RF signals.

IV. THE FET MODEL STRUCTURE

The model of the power transistor die comprises the gate and drain manifold structures that feed the voltages into the device, an extrinsic network of lumped element components that describes the resistance, inductance and capacitance attributable to the metal contacts, access regions of the transistor, etc., and the nonlinear model of the intrinsic part of the device: the channel region where the gain occurs.

A. Manifold Feed Structures

These metal pads are the locations where the bondwires land, and they subsequently feed the many gate and drain electrodes that make up the transistor itself. These manifold metallizations can often be modeled as simple capacitors, but for more sophisticated or accurate models we rely upon electromagnetic simulations of the metal, often including the bond-wire termination itself. The manifold can then be represented as a multi-port S-parameter network in the simulator.

B. Extrinsic Network

This network represents the part of the transistor required to connect the active channel region to the outside world. This includes: the resistive losses due to the access resistances

between the source and gate electrodes and the channel; inter-electrode capacitances; inductances of the metal electrodes, which can be several hundreds of microns in length in a typical power transistor. Several techniques have been described for identifying a suitable network, and for determining the parameter values [3]–[5]. Probably the most commonly used method is “Cold-FET”: here the transistor is biased into a passive condition, with the drain bias at zero voltage, and the gate is biased below threshold so that the device is switched off. In this condition the intrinsic transistor can be modeled effectively as a network of capacitors, enabling the extrinsic component values to be determined, using broadband S-parameter measurements [5].

C. The Nonlinear Model of the FET

As noted in the previous section, a bias-dependent linear FET model can be constructed from S-parameters made over the gate and drain bias voltage space. It is tempting to create a model by fitting two-dimensional functions to all of the equivalent circuit values, over the measured $\{V_{gs}, V_{ds}\}$ space, to obtain continuous variables of the resistances and capacitances with bias. However, this is *not* the same as having continuous variables for the model circuit parameters over an instantaneous voltage space: *it is not a large-signal model*. The reason for this is quite straightforward: the resistors and capacitors implemented in the circuit simulator are two-terminal components. The current flow in a resistor depends on the voltage across it, and the charge on a capacitor likewise depends up the time derivative of the voltage across its terminals. If we want to make these components dependent on two circuit voltages, we need to implement them as controlled sources. In most simulators, a ‘resistor’ whose instantaneous value depends on two voltages can be implemented as a controlled current source. A ‘capacitor’ whose instantaneous value depends on two voltages must be implemented as a controlled *charge* source, otherwise the law of charge conservation is broken [6]. Using simple two-terminal circuit components to implement the model in the simulator can lead to serious problems, such as lack of convergence in large-signal simulation, and the generation of unphysical DC currents [2], [7]. The nonlinear intrinsic part of the model structure that we adopt is shown in Fig. 4, [8], [9]. The current and charge source functions are found from integration of the appropriate small-signal parameters over the gate-drain voltage space, as shown in eqs. (1)–(4).

Writing the equations in this form retains the symmetry between real and imaginary parts of the Y-parameters, and the controlled current and charge sources. This integration can be performed numerically from the small-signal model parameter values, and stored in tabular form, or the integrated data fitted with a suitable nonlinear function.

D. Adding a Thermal Model

Power transistors dissipate a lot of heat; including temperature dependence into the model parameters is essential. Further, the information signals used in modern wireless

$$Q_g(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} [C_{gs}(v_{gs}, V_{ds0}) + C_{gd}(v_{gs}, V_{ds0})] dv_{gs} - \int_{V_{ds0}}^{V_{ds}} C_{gd}(V_{gs}, v_{ds}) dv_{ds} + Q_g(V_{gs0}, V_{ds0}) \quad (1)$$

$$Q_d(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} [C_m(v_{gs}, V_{ds0}) - C_{gd}(v_{gs}, V_{ds0})] dv_{gs} + \int_{V_{ds0}}^{V_{ds}} [C_{ds}(V_{gs}, v_{ds}) + C_{gd}(V_{gs}, v_{ds})] dv_{ds} + Q_d(V_{gs0}, V_{ds0}) \quad (2)$$

$$I_g(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} \text{Re}\{y_{11}(v_{gs}, V_{ds0})\} dv_{gs} + \int_{V_{ds0}}^{V_{ds}} \text{Re}\{y_{12}(V_{gs}, v_{ds})\} dv_{ds} + I_g(V_{gs0}, V_{ds0}) = \int_{V_{gs0}}^{V_{gs}} g_{gs}(v_{gs}, V_{ds0}) dv_{gs} + I_g(V_{gs0}, V_{ds0}) \quad (3)$$

$$I_d(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} g_m(v_{gs}, V_{ds0}) dv_{gs} + \int_{V_{ds0}}^{V_{ds}} g_{ds}(V_{gs}, v_{ds}) dv_{ds} + I_d(V_{gs0}, V_{ds0}) \quad (4)$$

Fig. 4. The schematic circuit for the large-signal model, showing the voltage-controlled gate charge and gate-source current sources, and the voltage-controlled drain charge and drain-source current sources.

communications signals have large peak-to-average ratios of the signal voltage or power: the dynamical response of the transistor's thermal behavior to these inputs must also be captured in the model. This means that an accurate dynamical electro-thermal model must be built. A simple way of including the thermal effects on the output current is to use a de-rating function on the drain current expression [10], [11]. This is effectively a wrapper around the drain current model, and can be expressed in the following way:

$$I_d = \frac{I_{d0}}{1 + \frac{(T - T_0)}{T_0}} = \frac{I_{d0}}{1 + \frac{R_{th} P_{avg}}{T_0}} \quad (5)$$

where R_{th} is the thermal resistance, which can be found from the difference between the drain current measured under isothermal (pulsed) conditions and DC, at a fixed substrate temperature. This is still a static expression. The instantaneous channel temperature is related to the instantaneous power, which is related to the average dissipated power through

$$\text{Heat Generation}(i_d, v_{ds}) = \text{Heat flow}(T - T_0) + \frac{d}{dt}(\text{Heat Storage})(T - T_0)$$

which becomes

$$P_{diss}(t) = \frac{(T - T_0)}{R_{th}} + C_{th} \frac{d}{dt}(T - T_0) \quad (6)$$

We have introduced a new thermal parameter, the thermal capacitance. This can be estimated from pulse profiling: observing the decay time of a pulse of drain current. To complete the thermal model, we must account for the variation with temperature of the threshold voltage. This acts in the opposite sense to the drain current de-rating, to produce a point in the drain current-gate voltage relationship that is independent of temperature: the zero-temperature coefficient point [12]. Including both thermal effects into the transistor model produces a dynamic electro-thermal model that can describe the transistor behavior under drive using modern communications signals.

V. VERIFICATION AND VALIDATION OF THE MODEL

After the model has been constructed and implemented in the simulator, we need to verify and validate it. Verification is the process by which the implementation of the model in the CAD tool is demonstrated to be consistent with the equations and topology of the model, and to ensure that it produces the expected results. Validation provides the assurance that the model has correct predictive qualities, and gives the circuit designers confidence in its use. Typical expressions of model validation include the comparison between model predictions and measured data, for measurements that were not used in the construction of the model itself. For power transistor models, a common example is the comparison between measured and modeled load-pull data.

Large-signal measurements usually form the focus of the validation set for power transistor models. Load-pull measurements, in which the device is presented with a wide range of complex loads and driven from small-signal conditions into compression, are generally used. Typically, only the fundamental signal is considered, but as more sophisticated power amplifier modes are considered, the harmonic load-pull performance is also important. In Fig. 5, we illustrate the validation of a model of a 900 MHz, 160 watt power transistor similar to that shown in Fig. 1, against swept power measurements made at the load impedance that produces the

Fig. 5. Measurement and simulations at 865 MHz of output power (a), IM3 (b), PAE (c), and G_T (d) when the source is matched and the impedance presented to the load is set of maximum PAE. © 2007 Cambridge University Press. Reprinted with permission

maximum power-added efficiency [2]. The model has been constructed following the principles outlined in this paper. The agreement between the model and the measured data is excellent, at the power levels under consideration.

VI. CONCLUSIONS

In this paper we have presented an outline of the measurement processes and analysis procedures that should be followed in order to construct an accurate, mathematically correct model for a power FET. We have stressed the need for accurate measurements, calibrations, during the device characterizations, and we have described the charge-conservative approach to the extraction of the large-signal nonlinear model. Electro-thermal effect have been included in a consistent manner. We have illustrated the success of our modeling approach by validation against large-signal measurements such as are typically used in RF power amplifiers.

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