On the Development of CAD Techniques Suitable for the Design of High-Power RF Transistors

Peter H. Aaen, *Member, IEEE*, Jaime A. Plá, *Member, IEEE*, and Constantine A. Balanis, *Life Fellow, IEEE*

Abstract—A full-wave modeling procedure was developed to simulate the package, bonding-wires and MOS capacitors used in the design of matching networks found within RF/microwave power transistors. The complex packaging environment was segmented into its constituent components and simulation techniques were developed for each component, as well as the inter-element coupling. An S-parameter test-fixture and package was developed which permits measurements of these types of devices. The simulation and measurement procedures were used to model various circuits. Measured S-parameters and those obtained using the full-wave methodology were in good agreement. Simulation results using an inductance only bonding-wire model were performed and differences between the S-parameters were observed. A detailed examination of the loss introduced by the matching network was performed and simulations and measurements are in good agreement.

Index Terms—High-power RF transistors, CAD techniques, bonding-wires, MOS capacitors

I. INTRODUCTION

HIGH-power RF amplifiers are employed within cellular base stations to provide sufficient power to enable communications between the base station and a multitude of handsets. The high-power capabilities are achieved via transistors that have very large gate peripheries, i.e., 200 mm. Consequently the input and output impedances of the transistor at the die tend to be very low; often less than 1Ω . In order to facilitate the ease of use of the transistor, as well as to allow for optimal performance, a matching circuit is constructed to transform the impedance at the die to a higher value. These matching networks are constructed with small diameter bonding-wires, often on the order of $25 \mu m$, and metal-oxide-semiconductor (MOS) capacitors. An illustration highlighting the internal construction of a typical RF power amplifier is provided in Fig. 1.

The matching networks formed by the bonding-wires and the MOS capacitors introduce very high Q resonances that provide the necessary impedance transformation. Slight changes to the bonding-wire arrays can result in frequency shifts of these resonances which adversely alter the characteristics of the matching network. In many applications bonding-wires are considered to be parasitic elements since they only serve as a means to provide a conductive interconnection between the leads of a the package and the semiconductor devices contained within it. However, within RF power transistors they are not parasitic elements as they are an integral part of the design.

The need for the development of a computer-aided design (CAD) methodology becomes apparent after viewing the internal three-dimensional construction of a power transistor, as

Fig. 1. The complexity of the internal construction of 2.1 GHz 90 W LDMOS transistor is illustrated. Note the intricate matching circuitry formed by the bonding-wires and MOS capacitors. Rows of parallel bonding-wires form arrays which interconnect the die, MOS capacitors and the package.

shown in Fig. 1. Unless accurate simulation techniques are developed, the design of the transistor is reduced to empirical tuning through re-manufacture, which is expensive and hinders time-to-market.

Development of CAD techniques for these devices is challenging since they can contain hundreds of bonding-wires, multiple active devices and several MOS capacitors all sealed within a single package. The coupling between various elements within the package further increases the complexity of the problem.

Significant attention has been directed towards the development of non-linear models for the active device [1]–[3]. However, little attention has been given to the development of modeling techniques for the complex matching networks which surround the active device. The techniques developed to date either employ measurement based approaches [4], [5] or a numerically efficient quasi-static algorithms [6], [7]. To date the computational burden imposed by the complex packaging environment has practically precluded the use of full-wave simulations.

In this paper, we present for the first time the development of a full-wave methodology to be used for the computer-aided design of matching networks employed within high-power RF transistors. Section II refines the CAD concept and outlines its key attributes. Section III discusses the simulation and measurement of the matching network constituent components. The measurement methodology used is presented in Section IV. Simulated and measured results are compared in Section V and the work concludes in Section VI.

II. COMPUTER-AIDED DESIGN CONCEPTS

Accurate and efficient simulations techniques are prerequisites for the development of RF/microwave circuit design environment. However, verifying the accuracy of these techniques is not straight-forward since only a few canonical geometries exist for which there are exact analytical solutions to Maxwell's equations. One method of verification often employed is to compare the results obtained through simulation with those from measurement. However, since both the simulation and measurement methodologies contain inherent errors, one set of data cannot be used to directly confirm the accuracy of the other.

Close examination of the generalized simulation process reveals potential sources of error [8]. One of the initial steps is to obtain an accurate description of the geometry for input into the simulator. Potential sources of error result from the measurement of the circuit dimensions and excessive de-featuring (removal of features deemed to be electrically small). Additionally, assumptions may be made about some dimensions which may be difficult to obtain such as dielectric or metal trace thickness.

Once the geometry has been extracted, a numerical technique is selected to solve Maxwell's equations. Approximations in the development or execution of the numerical technique are often made to reduce the required number of unknowns (i.e. infinite ground planes, surface impedances, etc.). The discretization method used as part of the numerical method is another source of potential error [9], [10].

Similarly, errors exist in the measurement process due to the mechanical tolerances of the test-fixtures, calibration kits and test-circuits. Additionally, errors may be created due to user error or they may be created during the calibration or measurement process. A schematic representing the potential errors involved with the measurements and simulations processes is outlined in Fig. 2.

Mathematically, the development of the CAD approach can be represented by an optimization which has a goal to minimize the difference between measured and simulated parameters of interest to a value below an acceptable tolerance. The difference is reduced through the iterative reduction of errors incurred throughout the simulation and measurement processes.

$$|S_{\text{simulated}} - S_{\text{measured}}| < \text{Tolerance} \quad (1)$$

Through judicious examinations and minimization of each potential error, it is possible to have a good comparison between simulated and measured results. Once an acceptable level of agreement has been obtained over the design space of interest, more emphasis can be placed on the simulator and circuit design can commence.

It is desirable that this optimization process be completed for the full transistor. However, the simulation of a full RF/microwave power transistor taxes the processing power of current computers to such a degree that full-electromagnetic simulation is not possible. However, through a systematic segmentation of the design space, the various sub-components can be completely characterized. This approach reduces both

Fig. 2. A flow-chart illustrating the potential sources of error in the measurement and simulation procedures used during the analysis of a circuit.

the complexity of the analysis and the computational load. Additionally, it facilitates device design since it allows models of the package, MOS capacitors and bonding-wires to be combined with other passive models from other simulators, and non-linear transistor models. Thus, a reductionistic study is well motivated.

III. SEGMENTATION AND COMPONENT SIMULATION

There are two major issues which exist when attempting to implement a segmentation approach to simulate a large complex circuit. The first is to devise a set of procedures which allows the individual circuit components to be separated from one another. The separation procedure must not perturb the behaviour of the components. That is, the component when analyzed must operate the same as it does within the larger device. The second issue is that any inter-element coupling, such as mutual inductance between arrays of bonding-wires, must be properly characterized.

The segmentation approach used in this work separates the elements from one another at reference planes where they connect to a microstrip transmission line. This implies that when any element is excited within a simulator it needs to be excited by a transmission line which has exactly the same characteristics as the one in the full device. As long as the circuits are excited identically, the electromagnetic fields on either side of the reference plane are the same and all of the electromagnetic simulation results can then be cascaded together.

A. Simulation of packages bonging-wire arrays

The performance of transistor is very sensitive to minor modifications in the shape of the bonding-wire array. In fact, it is so sensitive that the three dimensional profile and the spacing between adjacent wires are two of the main parameters which are used to control its performance.

A common problem to all simulation methods is how to accurately reproduce the 3-D geometry of the bonding-wire.

This not only complicates the numerical analysis, but it poses a problem to any simulation method as the geometry must be accurately captured prior its analysis. Several researchers have developed techniques to overcome this task through the use of scanning electron microscope or digital microscope photos [4], [6], [11], [12]. However, due to the size and complexity of a physically large packaged transistor and the difficulty and the time associated with obtaining photographs of sufficient quality, this method is not always applicable. In this work each device is measured and the bonding-wire profile is extracted using a high-power optical microscope outfitted with a precision-XYZ table. The amount of time required to measure a device is minimized by selecting a representative wire from each array and measuring its profile. The other bonding-wires in that array are assumed to have exactly the same profile.

The ability of the finite-element method to simulate the S-parameters of a set of bonding-wires within a packaged environment has been previously demonstrated [13]. For a large number of devices examined the S-parameters and calculated losses obtained through simulation compared well with measured data. An inductance-only bonding-wire model available within a commercially available circuit design package was also examined [12], [14]. It was shown that it is critical to properly account for the discontinuity between the bonding-wire array and the microstrip line to which it is attached. Additionally, the capacitance of the bonding-wire array was found to have a potentially significant role for arrays containing large numbers of bonding-wires [13].

The discontinuity between the array of bonding-wires and the microstrip is further complicated by the manufacturing requirements. For consistency during manufacturing, the bonding-wires are attached 100-200 μm behind the ending-edge of the microstrip. Therefore, no clear plane exists to segment the structure. While this discontinuity is easily included within the finite-element simulator, it presents a challenge to simulate it for an existing bonding-wire model. The assumption that the discontinuity can be characterized is implicit when existing bonding-wire models are used. In the work presented in this paper, the discontinuity is approximated by simulating a set of planar microstrips which connect to the microstrip. The set of coupled strips are de-embedded to the ending-edge of the microstrip [13].

The previous finite-element analysis concentrated on the analysis of circuits which included microstrips and bonding-wires and, due to their size, a segmentation approach was not required. However, in this work it is a necessity due to the complexity of the packaging environment. As previously stated, the segmentation will occur at locations where reference planes can be defined in the planar microstrip environment.

The segmentation approach can be highlighted and validated through the simulation of a package containing an array of bonding-wires connected between bonding-pads as illustrated in Fig. 3. The two microstrips on either side of the bonding-pads are used to excite the circuit within the finite-element based simulator. Once the simulation has been completed the microstrips will be de-embedded to the reference planes as

Fig. 3. A set of 16 bonding-wires connected between the leads of a package. The arrows indicate sections of transmission line which will be de-embedded from the simulated S-parameters. After de-embedding the reference planes will be as indicated.

Fig. 4. Segmentation of the packages and bonding-wires are microstrip reference planes. The reference planes for all segmented sections are indicated by the dashed lines. The arrows indicate sections of transmission line which will be de-embedded from the simulated S-parameters.

indicated in the Fig. 3. While the small physical size of the circuit allows the entire circuit to be characterized, the segmentation approach can be applied and the resulting S-parameters should be identical to those obtained from the simulation of the entire device. Illustrated in Fig. 4, the circuit shown in Fig. 3 is separated by segmenting the device at the ends of the bonding pads. In order to simulate the array of wires, it is attached to two microstrip transmission lines which have the same width of the bonding pad. These transmission lines, as before, are used to excite the array of bonding-wires within the simulator and are later de-embedded. As a result, the S-parameters contain the effects of the wires and the discontinuity between the microstrip and the array. This set of wires can then be cascaded with other circuit elements provided that they are excited with an identical transmission line when characterized. The segmentation process assumes that no discontinuity is close to the reference plane, otherwise higher-order modes present around the discontinuity may couple to the bonding-wires and perturb the results. As can be seen in Fig. 5, the S-parameters agree over the entire frequency of simulation, with very little difference between them.

B. Simulation of MOS capacitors

A MOS capacitor consists of a thin silicon dioxide (SiO_2) layer deposited on top of a heavily doped (conductive) silicon wafer. A metal pattern is created on to the top of the oxide to complete the formation of the capacitor. Metalization of the back of the wafer aids its attachment to a package flange. This system forms a metal-insulator-semiconductor (MIS)

Fig. 5. A comparison of the simulated input reflection coefficient for the device illustrated in Fig. 3. The device is simulated as an entire structure and using the segmentation procedure.

structure which is notoriously difficult to model due to the complicated frequency dependent behaviour introduced by the semiconducting substrate [15], [16]. An illustration of a cross section of a MOS capacitor is provided in Fig. 6. Depending on design requirements, the capacitance can range from 10-500 pF and it can be controlled by varying the thickness of the oxide and/or the area of the top metalization.

The layered structure of the MOS capacitor lends itself to simulation within a planar method-of-moments (MoM) based simulator. However, to be able to generate accurate simulation results with the simulator, the material parameters (i.e. conductivity, loss tangent, etc.) must be obtained. A wafer containing various ground-signal-ground (GSG) transmission lines and test capacitors was manufactured which contained sufficient structures to extract the material parameters of the materials used to construct the capacitor. An illustration of some of the transmission lines used during the extraction of substrate parameters is shown in Fig. 7.

The MOS capacitors examined had a substrate thickness of 125 μm , $\epsilon_r = 11.8$ and a conductivity of on the order of $1 \times 10^4 \text{ S/m}$, while the silicon dioxide layer had $\epsilon_r = 3.7$ and its thickness ranged from 1-2 μm (depending on the selected value of capacitance).

In order to demonstrate the agreement between simulation and measured S-parameters, several of the on-wafer structures were simulated. The agreement between simulated and measured results for the input reflection coefficient of two of the transmission lines is shown in Fig. 8. These transmission lines are 1000 μm in length, have a widths of 20 and 50 μm and are on top of a 1.38 μm oxide. Although not shown here, the remaining simulated and measured S-parameters show the same level of agreement.

In order to obtain the simulated S-parameters for a MOS capacitor used in a matching networks within the transistor, the top metalization of the capacitor is drawn and transmission lines equal to the width of the bonding-wire arrays connected to it are used to excite the capacitor, as illustrated in Fig. 9. In this manner the discontinuity between the bonding-wire array and the MOS capacitor is approximated as a step change in the width.

Fig. 6. A cross-section of a MOS capacitor is illustrated with typical dimensions. Bonding-wires are attached to the top metalization.

Fig. 7. GSG Transmission lines created on the same substrate as used for the MOS capacitors. The transmission lines are employed to aid the determination of the substrate material parameters. Vias connected to the grounds of the GSG pads permit a low-impedance connection through the conductive silicon to the back-side metallization of the wafer.

C. Coupling between Bonding-Wire Arrays

The arrays of bonding-wires within the package are often within close proximity, as illustrated in Fig. 1. Since the bonding-wire arrays form small conductive loops which carry current, it is expected that a significant amount of electromagnetic coupling occurs and that the coupling is inductive in nature. Once the inter-element coupling has been characterized, it can be accounted for within a circuit simulator through an appropriately placed mutual inductor.

The procedure used to obtain the mutual inductance builds upon the simulations outlined to characterize individual arrays of bonding-wires. Once each set of arrays has been simulated, the mutual coupling between the two arrays can be obtained by performing one additional simulation. In this simulation the circuit element to which both bonding-wire arrays are connected is replaced by a short circuit. This circuit is simulated and then the S-parameters of the bonding-wire arrays are de-embedded. The resulting transmission coefficient is the coupling between arrays and the mutual inductance, L_{mutual} , can be directly extracted once the S-parameters are converted to Z-parameters, where f is the frequency,

$$L_{mutual} = \frac{\text{imag}(Z_{21})}{2\pi f} \quad (2)$$

In general the computed mutual inductance between arrays of bonding-wires is a function of the bonding-wire geometry, the spacing between adjacent wires and distance between arrays.

The assumption that the coupling between arrays is due to mutual inductance is an approximation to the more generalized

Fig. 8. A plot of the simulated and measured input reflection coefficient of two $1000 \mu m$ transmission lines. The two transmission lines have widths of 30 and $50 \mu m$.

Fig. 9. A screen shot from the simulator used to simulate MOS capacitors. This capacitor is excited by two microstrip transmission lines which have widths equal to the width of the connecting array of bonding-wires. The transmission lines are de-embedded from the simulation results.

coupling exhibited between coupled transmission lines. Since the transmission lines are very small fractions of a wavelength, it is a reasonable assumption. However, if the frequency of operation is increased, the bonding-wires become electrically large, and the coupling is no longer due to just the mutual inductance. Additionally, the coupling will begin to depend on the impedance to which the arrays are terminated [17].

IV. MEASUREMENT METHODOLOGY

A measurement methodology was developed to obtain the S-parameters of test-circuits to which those obtained through simulation will be compared. The test-circuits will contain various combinations of microstrips, MOS capacitors and arrays of bonding-wires. Central to the test-fixture is a specially designed package which allows measurement reference planes to be rigorously established, as illustrated in Fig. 10. The metal carrier of these packages serves as the ground plane and as a mechanical support. The uniform ground-plane avoids any issues related to discontinuities in the ground-plane which occur when mounting transistor packages within test fixtures [13]. Bonded to this conductor is an alumina substrate which

Fig. 10. Illustrations of the structure used to characterize the step in the reference conductor.

contains a 50Ω transmission line and a bonding-pad. The microstrip lines allow the package to be connected to coaxial-to-microstrip launchers and the bonding-pads permit large numbers of bonding-wires to be connected to the microstrip. A large number of different sized packages can be constructed by varying the length of the metal carrier and width of the bonding-pads on the alumina substrate.

The packages are designed such that they can be inserted into a test fixture for measurement of the S-parameters. The metal carrier is bolted to a mechanical support and coax-to-microstrip launchers connect the cables of vector network analyzer to the alumina microstrips as illustrated in Fig. 11. This type of test fixture is frequently employed in measurements used to characterize RF and microwave transistors, and it was easily adapted for this study [18].

Once the device-under-test (DUT) is placed within the test fixture, a coax-to-microstrip launcher connects the cables of vector network analyzer to the alumina microstrips. Calibration of the test fixture is accomplished through a two-tiered thru-reflect-line (TRL) calibration [4]. The measurement reference planes are established at the ends of the narrow microstrip, just prior to the bonding pad, as illustrated in Fig. 10.

V. EVALUATION OF THE SIMULATION AND MEASUREMENT METHODOLOGIES

After the development of the aforementioned simulation and measurement techniques, it is necessary to test these methodologies on matching networks similar to those found within the transistor. To this end, several components containing various combinations of packages, bonding-wires and MOS capacitors were assembled, two of which are illustrated in Figures 12 and 13. While these devices are of reduced complexity, compared to that of a full transistor, Fig. 1, they are well suited for further investigation into the basic electrical behaviour of the constituent components and their interactions.

The first device, illustrated in Fig. 12, contains a 350 pF MOS capacitor mounted within a test-package. An array com-

Fig. 11. Exploded view of the test fixture.

Fig. 12. A 350 pF MOS capacitor bonded within a test package and connected by 2 arrays of bonding-wires.

posed of sixteen, $50\ \mu\text{m}$ diameter gold wires, each spaced by a centre-to-centre distance of $250\ \mu\text{m}$ connects each bonding-pad to the MOS capacitor. The second device, illustrated in Fig. 13, is composed of three, 22 pF MOS capacitors, interconnected with arrays of bonding-wires, with the final array shorted to the ground-plane.

The simulation techniques outlined in the previous section were employed to simulate each circuit component of the network and to obtain the mutual inductance between adjacent arrays of bonding-wires. The results were then combined together within a linear circuit-solver to obtain the S-parameters of the entire circuit. In addition, the same devices were simulated using the inductance-only bond-wire model, with the discontinuity between the planar transmission line elements and the arrays of bonding-wires approximated as previously mentioned. A selection of the simulated and measured S-parameters of each of these devices are plotted in Figures 14–17. The full-wave and measured results agree well over the entire frequency range with only minor differences. However, the simulations employing the inductance-only bonding-wire model are not in as close agreement. The differences are due to the approximation of the microstrip-bonding-wire array discontinuity and accuracy of the inductance obtained from the model.

An examination into the ability of the simulation methods to predict the measured losses present in the matching networks

Fig. 13. A high-Q resonator formed by three, 22 pF MOS capacitors connected with arrays of bonding-wires.

Fig. 14. A plot of the magnitude of the simulated and measured transmission coefficients for the device illustrated in Fig. 12.

was also performed. Since the structures contain very high conductivities and low-loss dielectrics, an examination of the S-parameter is not sufficient. Instead, a metric that is very sensitive to the loss must be used. One such is computation of the conservation or loss factor [13], and it can be computed via,

$$CF = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (3)$$

The conservation factor for the device illustrated in Fig. 13 is plotted in Fig. 18. As can be seen, the conservation factor for the measured and full-wave results compares very well over the entire frequency range. As expected from an examination of the S-parameter results, the simulations using the inductance-only bonding-wire model are shifted higher in frequency than the other results. Although not shown here, the conservation factor computed from the simulations and measured S-parameters from the device shown in Fig. 12 are in similar agreement.

VI. CONCLUSIONS

The complex packaging environment found within RF/microwave power transistors was analyzed through a systematic segmentation of its constituent components. Simulation and measurement techniques were developed to examine packages, bonding-wires and MOS capacitors.

Fig. 15. A plot of the phase of the simulated and measured transmission coefficient of the device illustrated in Fig. 12.

Fig. 17. The phase of the simulated and measured input reflection coefficient of the device illustrated in Fig. 13.

Fig. 16. The magnitude of the simulated and measured input reflection coefficient of the device illustrated in Fig. 13.

Fig. 18. A plot of the conservation factor computed from the simulated and measured S-parameters from the device illustrated in Fig. 13.

Specifically, the finite-element method and method-of-moments were found to be suitable numerical techniques for the electromagnetic simulation of these circuit elements.

Furthermore, these elements were cascaded together to form matching networks similar to those present within the transistor package. Measurements of several matching networks manufactured within packages were taken with a specialized test-fixture. Simulated S-parameters matched those obtained from measurement up to 10 GHz. In particular the losses of these circuits were examined through the computation of the conservation factor and measured and simulated results were in good agreement.

The investigation also revealed that a commercially available inductance-only bonding-wire model used in conjunction with a planar electromagnetic solver was able to simulate the low-frequency behaviour of a matching network. However, at higher frequencies significant differences were observed when compared with results obtained from measurement and full-wave analysis.

The analysis techniques developed as part of this work indicate that matching networks found within high-power RF/microwave transistors can be accurately simulated using

full-wave electromagnetic simulators. This development furthers the evolution of a computer-aided design methodology.

ACKNOWLEDGMENT

The authors would like to thank Dan Lamey, Margaret Szymanowski and Daniel Chan for their work related to determining the material parameters and developing a simulation methodology for the MOS capacitors.

REFERENCES

- [1] W. R. Curtice, J. A. Plá, D. Bridges, T. Liang, and E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs," in *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, Anaheim, CA USA, June 1999, pp. 419–422.
- [2] D. E. Root, S. Fan, and J. Meyer, "Technology-independent large-signal FET models: a measurement-based approach to active device modeling," in *Proc. 15th Automated RF and Microwave Measurements Society (ARMMS) Conference*, Bath, UK, Sept. 1991, pp. 1–21.
- [3] M. Guyonnet, R. Sommet, R. Quere, and G. Bouisse, "Non-linear electro thermal model of LDMOS power transistor coupled to 3D thermal model in a circuit simulator," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, Toulouse, France, Sept. 2003, pp. 11–14.
- [4] T. Liang, J. A. Plá, P. H. Aaen, and M. Mahalingam, "Equivalent-circuit modeling and verification of metal-ceramic packages for RF and microwave power transistors," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, pp. 709–712, June 1999.

- [5] K. Goverdhanam *et al.*, "Modeling high power RF LDMOS amplifiers," in 2004 *IEEE MTT-S Int. Microwave Symp. Dig.*, Fort Worth, TX USA, June 2004, pp. 1069–1072.
- [6] T. Johansson and T. Arnborg, "A novel approach to 3-D modeling of packaged RF power transistors," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, pp. 760–768, June 1999.
- [7] K. Mouthaan, "Modeling of RF high power bipolar transistors," Ph.D. dissertation, Delft University of Technology, Delft, Netherlands, 2001.
- [8] J. T. Aberle, "Finite difference methods: accuracy, consistency, stability and convergence of solutions," Feb. 2000, personal class notes.
- [9] E. H. Lenzing and J. C. Rautio, "A model for discretization error in electromagnetic analysis of capacitors," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, pp. 162–166, Feb. 1998.
- [10] J. C. Rautio, "The microwave point of view on software validation," *IEEE Antennas and Propagation Magazine*, vol. 38, pp. 68–71, Apr. 1996.
- [11] X. Qi *et al.*, "A fast 3D modeling approach to electrical parameters extraction of bonding wires for RF circuits," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 480–488, Aug. 2000.
- [12] K. Mouthaan *et al.*, "Microwave modeling and measurement of the self- and mutual inductances of coupled bondwires," in *IEEE Bipolar Circuits Technology Meeting*, Minneapolis, MN USA, 1997, pp. 166–169.
- [13] P. H. Aaen, "Simulation and modeling of matching networks within RF/microwave power transistors," Ph.D. dissertation, Arizona State University, Tempe, AZ, 2005.
- [14] *Agilent's Advanced Design System version 2002c, Circuit Component, System Models*, Palo Alto, CA USA, Sept. 2002, ch. 4, pp. 10–27.
- [15] H. Guckel, P. A. Brennan, and I. Palocz, "A parallel-plate waveguide approach to micro-miniaturized, planar transmission lines for integrated circuits," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT15, pp. 468–472, Aug. 1967.
- [16] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on $Si - SiO_2$ system," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT19, pp. 869–881, Nov. 1971.
- [17] E. M. T. Jones and J. T. Bolljahn, "Coupled-strip-transmission-line filters and directional couplers," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT4, pp. 75–81, Apr. 1956.
- [18] G. D. Vendelin, A. M. Pavio, and U. L. Rhode, *Microwave circuit design using linear and non-linear techniques*, 2nd ed. New York, NY USA: Wiley-Interscience, 1992, ch. 5, pp. 313–334.

Peter H. Aaen (S93–M97) received the B.A.Sc. degree in engineering science, the M.A.Sc. degree in electrical engineering both from the University of Toronto, Toronto, ON., Canada, and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, in 1995, 1997 and 2005, respectively. In 1997, he joined the Wireless Infrastructure Systems Division, Semiconductor Products Sector, Motorola (now Freescale Semiconductor Inc.), in Phoenix, Arizona. His current work focuses on the development and validation of microwave transistor models and passive components. His technical interests include calibration techniques for microwave measurements and the development of package modeling techniques.

Jaime A. Plá (S'87–M'91) was born in Puerto Rico, in 1969. He received the B.S. degree in electrical engineering from the University of Puerto Rico, Mayagüez, in 1991, and the M.S. degree in microwave engineering from the University of Massachusetts at Amherst, in 1993. In 1991, he joined the Microwave Semiconductor Laboratory, Research Division, Raytheon, Lexington, MA. While with Raytheon, he was primarily involved with the development of microwave measurement techniques and linear and nonlinear models for monolithic-microwave integrated-circuit (MMIC) semiconductor devices such as GaAs MESFET's PHEMT's, and HBT's. In 1995, he joined the Wireless Infrastructure Systems Division, Semiconductor Product Sector, Motorola (now Freescale Semiconductor Inc.), Phoenix, AZ, where his current work is centered on the development of high-power RF electro-thermal device models for LDMOS devices. Other areas of current interest are the development of package modeling techniques and modeling of passive components, as well as techniques for the measurement of electrical and thermal transistor characteristics related to small- and large-signal modeling extraction and validation.

Constantine A. Balanis (S62–M68–M74–F'86–LF'04) received the B.S.E.E. degree from Virginia Tech., Blacksburg, the M.E.E. degree from the University of Virginia, Charlottesville, and the Ph.D. degree in electrical engineering from Ohio State University, Columbus, in 1964, 1966, and 1969, respectively. From 1964 to 1970, he was with the National Aeronautics and Space Administration (NASA) Langley Research Center, Hampton, VA. From 1970 to 1983, he was with the Department of Electrical Engineering, West Virginia University, Morgantown. Since 1983, he has been with the Department of Electrical Engineering, Arizona State University (ASU), Tempe, where he is now Regents Professor. He is the author of *Antenna Theory: Analysis and Design* (New York: Wiley, 2005, 1997 and 1982) and *Advanced Engineering Electromagnetics* (New York: Wiley, 1989). His research interests are in low- and high-frequency computational methods for antennas and scattering, smart antennas for wireless communication, and high intensity radiated fields (HIRF). Dr. Balanis received the 1987 Graduate Teaching Excellence Award, School of Engineering, ASU, 1989 IEEE Region 6 Individual Achievement Award, 1992 Special Professionalism Award from the IEEE Phoenix Section, 1996 Arizona State University Outstanding Graduate Mentor Award, and 2000 IEEE Third Millennium Medal, an Honorary Doctorate from the Aristotle University of Thessaloniki (AUTH) in 2004, and the 2005 Chen-To Tai Distinguished Educator Award of the IEEE AP Society. He served as Associate Editor of the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION from 1974–1977 and IEEE TRANSACTIONS ON GEOSCIENCE AND REMOTE SENSING from 1981–1984. He was Editor of the Newsletter for the IEEE Geoscience and Remote Sensing Society from 1982–1983, Second Vice-President of the IEEE Geoscience and Remote Sensing Society in 1984, Chairman of the Distinguished Lecturer Program from 1988–1991, and a Member of of the IEEE Antennas and Propagation Society AdCom from 1993–1995 and 1997–1999. Presently he is a Distinguished Lecturer for the IEEE Antennas and Propagation Society.