Temperature effects in complementary inverters made with polysilicon source-gated transistors

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Abstract — Through their high gain and low saturation voltage, source-gated transistors (SGTs) have applications in both analog and digital thin-film circuits. In this study we show how we can design SGT-based logic gates which are practically unaffected by temperature variations. We discuss design characteristics which ensure reliable operation in spite of SGT temperature dependence of drain current, and their implications for manufacturability and large signal operation.

Key words — Schottky barrier, thin-film transistor, source-gated transistor, complementary logic gate, gain, noise margin, temperature effects, polysilicon

I. INTRODUCTION

Source-gated transistors (SGTs) have remarkable properties for thin-film digital circuits [1], as well as for analog applications [2-4]. Their use results in noise-tolerant logic gates, high gain current sources, high noise immunity, and superior power efficiency, and such devices have been demonstrated in a variety of technologies [5-7]. Unlike the rapidly evolving ULSI CMOS, advances in large area thin-film transistor architecture have been limited, but by basing certain aspects of circuit design on SGTs, major progress can be achieved.

We have previously showed that complementary SGT inverters made using polysilicon device can have exceptionally large gain and superior noise margin due to the low dependence on drain bias of drain current and to low-voltage saturation [1].

Here, we show the versatility of complementary SGT-based logic, with excellent performance against temperature despite potentially the large temperature dependence (TD) of SGT drain current. We focus on the polysilicon technology for the following reasons: the capability of the SGT device architecture to effectively suppress the kink effect [8-11] which is detrimental to both analog and digital operation; the ability to create complementary circuits (i.e. both *n*- and *p*-

type devices) with reduced stand-by power and small component count in comparison to unipolar logic [12-17] which is used out of necessity in many emerging technologies. Renewed relevance of polysilicon both through material and technology advances [18-21] and applications [22-25] makes it a rapidly progressing technology.

We support our findings using measurements on polysilicon SGTs and calibrated simulations using the Silvaco Atlas mixed-mode tools [26].

II. POLYSILICON SOURCE-GATED TRANSISTORS

A. Fabrication and modeling of source-gated transistors

Figure 1 shows a schematic cross-section and an optical micrograph of an *n*-type poly-Si source-gated transistor (SGT).

Figure 1. Top - optical micrograph of self-aligned polysilicon SGT ($W = 50\mu\text{m}$, $d = 10\mu\text{m}$, $S = 10\mu\text{m}$, $t_s = 40\text{nm}$, $t_i = 300\text{nm}$ equivalent oxide thickness, $h = 120\text{nm}$, $l = 2\mu\text{m}$); bottom - schematic cross-section of the self-aligned (gate-drain) SGT with field plate.

Bottom-gate, staggered electrode devices have been fabricated on glass substrates in a conventional LTPS process using excimer laser crystallization of silicon and self-aligned drain implants by back exposure using the gate as a mask [2] (Fig. 1). After patterning the Cr gate using photolithography, 200nm of SiN_x and 200nm of SiO₂ were deposited to act as gate insulator (300nm equivalent oxide thickness). 40nm hydrogenated amorphous silicon was deposited, baked at 450°C, and laser crystallized to form the active layer, which was passivated with 120nm of SiO₂. Top contacts were defined by opening windows in the top insulator and depositing Cr/AlTi/Cr. The metal was patterned photolithographically to form overhangs which served as field relief structures. The drain ohmic contact was formed by n⁺⁺ P doping. The semiconductor had varying levels of bulk doping for threshold control. Annealing of dopants was performed at 550°C.

Polysilicon SGTs have desirable properties such as low saturation voltage (V_{SAT}) and flat saturated curves (Fig. 2) [2, 4] with suppression of kink effect up to very high drain voltages, tolerance to geometrical variations during fabrication and drain current practically independent on source-drain gap (d in Fig. 1). Moreover, the flatness of the saturated characteristics can be maintained even for a short d with adequate (and easy to fabricate) field relief structures [27-30].

These devices were the starting point of our circuit simulations with Silvaco Atlas [26]. After fitting the measured curves, the structure was optimized ($t_i = 100\text{nm}$; $t_s = 40\text{nm}$; field relief plate [30] $h = 30\text{nm}$, $l = 1\mu\text{m}$; $d = 5\mu\text{m}$; source barrier $\phi_{B0} = 0.45\text{eV}$) to achieve low voltage operation with small positive V_T . The simulations performed were two-dimensional and used the cross section of the device (implied width $W = 1\mu\text{m}$) divided in a dynamically spaced grid, with coarser spacing in the middle of the s/d electrode gap and at device edges, and finer at the source edge in the x direction and at the semiconductor interfaces in the y direction.

The drain contact was defined as ohmic. The source contact comprised a Schottky barrier to electrons, achieved by enabling the respective flags (*barrier*, *surf.rec*) and setting the work function of the source electrode to 4.62eV, 0.45eV higher than the electron affinity of the semiconductor. Barrier lowering was enabled by setting $\alpha = 4\text{nm}$, $\beta = 1$, $\gamma = 1$, which includes a component proportional to electric field, along with the image force.

Material parameters were chosen to reflect a standard polysilicon process and were set to Atlas defaults. Ambient temperature was kept constant for each simulation run.

The p -type device was defined using the same material parameters and geometry. The nominal barrier of $\phi_{B0} = 0.45\text{eV}$ for holes was generated by choosing the source work function as 0.45eV lower than the sum of semiconductor electron affinity and its band gap. Transfer characteristics for both n -type and p -type devices are identical to Fig 2d in [1].

Circuit simulation was performed using the Atlas mixed-

mode capability. The inverter was created using SPICE-like syntax for connecting the components, and defining the n -type and p -type devices physically as described above. Transient simulation used the capacitances extracted automatically from the physical simulation.

Figure 2. Measured output characteristics of an enhancement-mode polysilicon SGT; ($W = 50\mu\text{m}$, $d = 10\mu\text{m}$, $S = 4\mu\text{m}$, $t_s = 40\text{nm}$, $t_i = 300\text{nm}$ equivalent oxide thickness, $h = 120\text{nm}$, $l = 2\mu\text{m}$).

B. Temperature effects in SGTs

SGT drain current can be temperature dependent due to its operation based on the reverse-biased source barrier. Current may increase rapidly with temperature, and along with it, the output conductance ($g_d = \partial I_D / \partial V_D$) (Fig. 3), essential for high intrinsic gain ($A_V = g_m / g_d$, where $g_m = \partial I_D / \partial V_G$).

By choosing an appropriate source length (S) we can switch from an operating mode which relies to barrier lowering at the edge of the source, with a high TD (short S), to a mode in which the drain current is dominated by the current from the bulk of the source, with a lower dependence (long S) [31, 32] (see Fig. 1 for schematic composition of drain current). Fig. 4 illustrates the change in temperature-related behavior for extreme values of S . The device with a long source has a larger drain current (injected from a larger source area). Significantly, the current originating from the bulk of the source has a lower TD than that of current being injected from the edge of the source electrode and, as a result, the overall temperature dependence of the drain current is lower for longer values of S [31]. This can be explained by the distinct current control processes for I_1 and I_2 : reverse saturation current of a Schottky contact for I_1 ; and a resistive effect as I_2 travels across the semiconductor width, through the accumulated channel and across the depletion region under the edge of the source for I_2 . Fig. 5 shows the gradual transition from one mode of operation (dominated by injection from the edge of the source, high TD) to another (dominated by injection from the bulk of the source, low TD) with increasing S . Measured data for two source lengths are presented in the inset.

Figure 3. The output conductance, $g_d = \partial I_D / \partial V_D$, of the SGT increases as drain current rises with temperature. $S = 5 \mu\text{m}$.

Figure 4. Transfer characteristics of the simulated SGT (*n*-type) used in the complementary inverter, at two temperatures and two values of S . The current increase with temperature is less in the device with a longer source

Figure 5. Relative increase of drain current when temperature is changed from 300K to 360K. SGT source length (S) influences drain current sensitivity to temperature: a transition occurs from the first mode of operation (high activation energy, high electric field) to the second mode (low activation energy, low field). Inset: measured dependence of current on temperature and source electrode length on polysilicon transistors.

As S is increased, the saturation voltage does not change (Fig 6a) as it depends on the electrostatics of the depleted semiconductor at the source edge and of the insulator for a given bias condition. This is a useful property which can be exploited in the fabrication of both analog and digital SGT

circuits with lower TD when S is used as a design parameter. Fig 6a also shows that for very long S the current saturates with S due to the two-dimensional potential distribution in the source region of the semiconductor [5].

Figure 6. a) Simulated SGT output characteristics for a logarithmic change in (S) from $0.2 \mu\text{m}$ to $100 \mu\text{m}$ at 300K and for device width $W = 1 \mu\text{m}$. $V_G = 5\text{V}$. Note that the saturation voltage does not change; b) the output characteristic becomes more rounded as the current increases at higher temperature ($S = 4.5 \mu\text{m}$).

Likewise, there is only a small saturation voltage shift to higher voltages when temperature increases (Fig. 6b). This is most likely due to the fact that the current density injected at the source is higher as the temperature increases and this larger current follows the envelope imposed by the conductivity of the accumulation channel between source and drain for the respective biasing condition.

III. SGTs IN DIGITAL CIRCUITS

A. Complementary SGT inverters

The electrical characteristics of polysilicon SGTs have been fitted through physical device simulations using Silvaco Atlas [1]. After optimizing the structure for lower voltage operation and positive threshold voltage (see Section II A above), an equivalent *p*-type device was modelled and complementary inverters (Fig. 7) were constructed using the mixed-mode environment of Atlas in which TCAD and SPICE-type simulations can be concurrently performed.

Figure 7. Schematic showing complementary inverter configuration. A.C. simulations were performed using an identical inverter as load at node OUT.

The complementary inverters based on polysilicon SGTs show excellent d.c. switching characteristics (Fig. 8) with high noise margin and gain (Fig. 9), and lower power-delay

product [1] compared to the equivalent FET circuit. These properties recommend SGTs as suitable building blocks for reliable, efficient and easy-to-fabricate large-area digital circuits. Source barrier heights for *p*- and *n*-type SGTs were chosen so that drain currents would be comparable, and device widths were $W_p = 2\mu\text{m}$ and $W_n = 1\mu\text{m}$, in keeping with the conventional sizing scheme of silicon-based logic components.

Figure 8. Simulated transfer curves for FET and SGT complementary inverters in polysilicon. Low saturation voltage and flat saturated characteristics allow the SGT circuit to respond closer to ideal than the FET inverter. $S = 5\mu\text{m}$. After [1].

Figure 9. Comparison of complementary inverter gain when made with FETs and SGTs - simulation. $S = 5\mu\text{m}$.

B. SGT inverter performance; temperature and source geometry considerations

In this study we show that SGT TD is not detrimental to complementary inverter operation. Figures 10 and 11 illustrate the noise margin (NM) and inverter gain for two temperatures and different values of S for complementary SGT inverters.

We see that temperature is having little or no adverse effect on SGT inverters, regardless of S . NM (definition incurrent context in the inset of Fig. 10) decreases slightly at high temperature as a result of rounding of output curves around V_{SAT} (Fig 6b). On the other hand, the inverter gain increases with temperature. We explain this behaviour through the simultaneous increase of g_d and g_m as the drain

current becomes larger at higher temperature. However, the increase in g_d is proportionally smaller, due to the saturation mechanism of the SGT and also to field plate functionality, resulting in higher intrinsic gain.

Moderate increases in both metrics are achieved when S increases, particularly in the few-microns range. The SGT circuits significantly outperform the FET equivalent, plotted for comparison in both Fig. 10 and Fig. 11.

Increasing source length benefits the gain and noise margin, but more importantly both NM and inverter gain are not detrimentally affected by increased temperature, regardless of the value of S , supporting the conclusion that SGT logic circuits are robust and reliable, despite potentially large TD of device drain current.

Source area, directly linked to S , does, however, impact the switching characteristics, through contributions to gate capacitance. The fall time (t_F) for a SGT inverter loaded with an identical circuit is shown in Fig. 12. An optimum value for S exists, since for long S the current does not increase linearly with S (Fig 6a) and for short S the current is impractically small. For this setup, the optimum range is $S = 10 - 30\mu\text{m}$, which changes only slightly with temperature. This is a useful span of values, considering that conventional polysilicon technologies have design rules in which metal-semiconductor (doped) contact regions are approximately of this size.

Figure 10. Comparison of FET and SGT (different S values) complementary inverter noise margin. $V_D = 5\text{V}$. The degradation with temperature is minimal. Inset – total noise margin calculation, after [1].

Fig. 13 shows that the energy expended per switching event increases linearly with S . The current injected increases with S , but so too does the capacitance which needs to be charged when a similar stage is used as a load. This further supports the preference for a small S .

Fig. 14 illustrates the interrelation between various metrics obtained by changing S ; NM, gain and fall time all improve as S increases to the optimum. At high temperature, fall time, related to switching speed, is lower, as the current

increases; gain also improves slightly. Higher gain is achieved simultaneously with faster switching and long S favors both. Noise margin does not improve significantly for very long S . Where switching speed is not important, designing for high gain does not compromise the noise margin. For the fastest switching, a value of S close to the optimum should be used, with minimal penalty in noise margin.

Figure 11. Comparison of FET and SGT (different S values) complementary inverter gain. Gain increases in the SGT inverter due to the rise in drain current (and g_m) with temperature.

Figure 12. Fall time (to 10% of V_{DD}) for the complementary SGT inverter, against S and temperature.

IV. CONCLUSIONS

Complementary SGT inverters have properties which allow a significant move forward in application performance and robustness for digital large area electronics, with significantly higher gain and noise margin than equivalent FET circuits, as shown in our polysilicon study [1].

Despite the potentially high temperature dependence of SGT drain current, we show that d.c. digital circuit performance does not degrade with temperature. The length of the source electrode, S , is a parameter which can be

changed in order to lower TD. We show that an optimum value of S , taking into account both behavior against temperature and switching speed, exists in the 10-micron range. This is practical from a technological point of view. As the current is controlled at the source, the source-drain gap can be made short without a large penalty in gain, especially for long S . As such, choosing the optimum S and minimum source-drain separation will not result in a compact footprint for SGT-based circuit blocks, making this technology easy to implement.

With excellent stability, tolerance to fabrication variability, simplicity of structure, and energy efficiency, SGTs are very promising components for the next generation of robust, high-gain large area thin-film digital and analog circuits, suggesting a potential increase in yield and consistency of performance.

Figure 13. Energy per switching event vs. S for the complementary SGT inverter.

Figure 14. Illustration of the relationship of the performance characteristics of the complementary SGT inverter achieved by changing S .

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