SiGe HBTs on Bonded SOI Incorporating Buried Silicide Layers

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Abstract—A technology is described for fabricating SiGe heterojunction bipolar transistors (HBTs) on wafer-bonded silicon-on-insulator (SOI) substrates that incorporate buried tungsten silicide layers for collector resistance reduction or buried groundplanes for crosstalk suppression. The physical structure of the devices is characterized using cross section transmission electron microscopy, and the electrical properties of the buried tungsten silicide layer are characterized using sheet resistance measurements as a function of bond temperature. Possible contamination issues associated with the buried tungsten silicide layer are investigated by measuring the collector/base reverse diode tics. A resistivity of $50 \mu\Omega\text{cm}$ is obtained for the buried silicide layer for a bond anneal of 120 min at 1000°C . Collector/base reverse diode tics show a voltage dependence of approximately $V^{1/2}$, indicating that the leakage current is due to Shockley–Read–Hall generation in the depletion region. Fitting of the current–voltage tics gives a generation lifetime of 90 ns, which is as expected for the collector doping of $7 \times 10^{17} \text{ cm}^{-3}$. These results indicate that the buried tungsten silicide layer does not have a serious impact on junction leakage.

Index Terms—Buried layer, groundplane, SiGe heterojunction bipolar transistors (HBTs), silicon-on-insulator (SOI), tungsten silicide, wafer bonding.

I. INTRODUCTION

OVER the past ten years SiGe heterojunction bipolar transistors (HBTs) have come of age as RF devices in a range of commercial SiGe BiCMOS technologies [1]–[6]. These technologies typically offer an SiGe HBT with a value of f_T and f_{max} around 100 GHz, and a range of passive components specifically targeted at RF circuit design [7]. A wide range of RF and mixed-signal circuits have been designed in SiGe BiCMOS technology, including low-noise amplifiers, power amplifiers, mixers, voltage controlled oscillators, synthesizers, and high-speed analogue-to-digital and digital-to-analog converters [2], [8]. Even higher frequencies of operation are possible with SiGe HBTs, as can be seen from state-of-the-art

values of f_T of around 300 GHz [9]. This opens up a second application area in optical fiber communication systems operating at 10, 20, and 40 Gb/s [10]. A typical product here would be optical fiber to the curb or to the home. Silicon bipolar integrated circuits have already been reported for 10 Gb/s [11] optical communication systems and research is underway on both Si bipolar and SiGe heterojunction bipolar circuits for 20 [12] and 40 Gb/s [10], [13], [14] systems. A variety of circuits have been realized, including dividers, multiplexers, demultiplexers, preamplifiers, and decision circuits [10].

Recently, there has been increasing interest in SiGe HBT on SOI technology [15]–[19], which allows the complete dielectric isolation of the device by combining a buried oxide with deep trench isolation. This approach reduces parasitic capacitances, leakage currents and the devices size. Furthermore, the SOI substrate eliminates parasitic substrate transistors and latchup and has the ability to reduce crosstalk, particularly when combined with buried groundplanes [20], [21]. These benefits make SiGe HBTs on SOI attractive for mixed-signal RF applications.

Collector resistance is a key issue in SiGe HBTs on SOI. Buried silicide layers in SOI have been demonstrated to offer low resistance contacts and near ideal tics in silicon diode structures [22]. These substrates have been proposed as a solution to the collector resistance problem [22]–[24] for a variety of device applications. However, this concept has not yet been implemented in bipolar technologies and contamination issues associated with the use of buried silicides in front-end processing have not been investigated. In this paper, we describe the fabrication and electrical tics of SiGe HBTs on bonded SOI incorporating a buried tungsten silicide collector layer to reduce the collector resistance. Process options for combining buried silicide collector layers with buried groundplanes are also considered. Contamination issues from the buried silicide layers are investigated by characterization and modeling of the reverse collector/base current–voltage tics.

II. SILICIDE SOI HBT CONCEPT

Fig. 1 shows the concept of the silicide SOI (SSOI) SiGe HBT technology. Key features of the technology are the inclusion of a buried silicide layer above the buried oxide layer for reduction of collector resistance and a buried silicide groundplane below the buried oxide layer for crosstalk suppression [20]. The n+ buried layer is needed in the SSOI process to prevent the formation of a Schottky contact between the buried silicide and the silicon collector. The technology also features complete dielectric isolation of the transistor island using a combination of deep trench isolation and the buried oxide layer.

Manuscript received September 9, 2004; revised December 17, 2004. This work was supported by the Engineering and Physical Sciences Research Council (EPSRC). The review of this paper is arranged by Editor J. N. Burghartz.

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Digital Object Identifier 10.1109/TED.2005.843872

Fig. 1. Schematic cross section of SiGe HBT on wafer-bonded SOI with buried silicide collector layer and buried silicide groundplane.

Fig. 2. Illustration of types of SOI collector. (a) SOI with buried n+ layer. (b) SOI with buried silicide collector layer (SSOI). (c) SOI with buried silicide collector layer and buried silicide groundplane (GPSSOI).

In the technology in Fig. 1, a silicon collector is grown using selective epitaxy (n-Si SEG) after completion of the wafer bonding processes in order to provide a well controlled collector doping profile. The selective silicon collector is grown in the same growth step as the nonselective growth of the SiGe base (p+ SiGe NSEG) and silicon cap layer. This combined selective and nonselective growth process will give good control of the collector profile without requiring a separate collector epitaxy process. Further details of the combined selective and nonselective epitaxy process are given in [25].

III. WAFER BONDING PROCESSES

Fig. 2 shows three process options for the SOI collector structure, including the SOI collector with an n+ buried layer (SOI) reported previously [17], the silicide SOI collector with a buried silicide layer (SSOI), and the SSOI collector combined with a buried silicide groundplane (GPSSOI). In the SOI process, a standard n+ buried layer is included above the buried oxide layer to reduce collector resistance, whereas in the SSOI process, a buried tungsten silicide layer, combined with an n+ buried layer is included above the buried oxide layer to reduce collector resistance. In the GPSSOI process, a buried silicide groundplane

below the buried oxide is combined with a buried silicide collector above the buried oxide.

Fig. 3(a) shows the process flow required to produce a basic SOI collector. The process begins with a $5 \times 10^{15} \text{ cm}^{-2}$, 80 keV arsenic implant into the active silicon wafer to form an n+ buried layer. A thermal oxide, $0.5 \mu\text{m}$ thick, is grown on the handle wafer, the implanted active and the oxidized handle are bonded at room temperature. After inspection the bonded pair receive a high temperature anneal at 1000°C for 2 h in a nitrogen environment in order to increase bond strength. This anneal is the largest thermal budget which will be experienced by the substrate during HBT manufacture. Previous work has established the stability of the tungsten silicide during thermal processing. The silicide layer was shown to be free from agglomeration effects for 2-h anneal schedules up to 1100°C [26]. The active silicon substrate is then ground to $6\text{--}8 \mu\text{m}$, the final SOI thickness of $1.5 \mu\text{m}$ is achieved by precision polishing of the ground SOI layer.

In the silicide SOI process (SSOI) it is advantageous to have a thermal oxide as the buried oxide layer, and Fig. 3(b) shows how this can be achieved. After the n+ buried layer is implanted in the active wafer a tungsten silicide (WSi_x) layer, $t \sim 200 \text{ nm}$,

Fig. 3. Process flows for (a) SOI collectors with buried n+ layer and (b) SOI collectors with buried silicide layer.

is deposited by chemical vapor deposition (CVD) at 370 °C. A polysilicon layer $t \sim 0.6 \mu\text{m}$ is then deposited on the tungsten silicide. This polycrystalline silicon layer is polished to produce a bondable surface, typically removing $0.3 \mu\text{m}$. The active silicon substrate is then bonded at room temperature to the oxidized handle wafer. The SOI is thinned as before while compensating for the presence of the silicide/polysilicon layers.

Fig. 4 shows how a buried silicide collector layer above the buried oxide layer can be combined with a silicide groundplane below the buried oxide layer (GPSSOI). The tungsten silicide layer required for the groundplane is deposited on the handle wafer using chemical vapor deposition as shown in Fig. 4(a). If necessary, the groundplane can be patterned using lithography and dry etching, as shown in Fig. 4(b). This is typically necessary beneath inductors to break up magnetically induced eddy currents. In order to incorporate a patterned ground plane into an SOI substrate a polysilicon layer is deposited over the patterned silicide layer and planarized using CMP, Fig. 4(d). A low-pressure chemical vapor deposition tetraethoxysilane oxide layer is then deposited over the planarized polysilicon as shown in Fig. 4(e) the deposited oxide will be the buried oxide (BOX) of the final SOI structure. This oxide layer is then polished to produce a bondable surface and is bonded to the active silicon substrate Fig. 4(f). After bonding the active wafer is thinned as before.

IV. RESULTS AND DISCUSSION

Fig. 5 shows a cross section TEM image of the basic SOI bonding process at the completion of the device processing. The buried oxide layer can be seen as a dark band in the bottom left hand corner of the picture and shows good contact with the active silicon wafer. The thickness of the buried oxide layer

is $0.51 \mu\text{m}$. The active silicon collector layer above the buried oxide layer has been ground and polished to a final thickness of $1.4 \mu\text{m}$. The selectively grown Si collector can be seen in the oxide window above the thinned active silicon layer. The nonselective SiGe base can be seen as a thin, dark line above the silicon collector, and is polycrystalline over the field oxide layer. The polysilicon emitter can be seen above the emitter Si cap layer and the top layer is a silicon dioxide layer deposited prior to contact and metal formation.

Fig. 6 shows a transmission electron microscope (TEM) cross section of the combined SEG/NSEG growth process. The selective Si layer aligns very well with the top of the field oxide layer, thereby giving a very planar surface on which the SiGe base can be grown. The nonselective growth process gives single-crystal material over the collector and polycrystalline material over the field oxide, which is later used for the base contact. The thickness of the polycrystalline layer is thinner than the equivalent single-crystal layer, indicating that an incubation time is required before polycrystalline material is deposited on the field oxide. The SiGe base can be seen as a dark layer sandwiched between two lighter silicon layers. The original growth interface can be seen as a dark line at the same depth as the bottom of the field oxide and is a significant distance away from the collector/base junction. Thus collector/base leakage currents will not be present due to the intersection of the growth interface with the collector/base depletion region. The fringes at the top corner of the oxide window indicate the presence of strain in the TEM foil. The location of the fringes at the top of the window suggests that the selective epitaxy is the origin of the strain.

Fig. 7 shows a cross-sectional TEM of the as-fabricated SOI substrate incorporating the buried tungsten silicide (WSi_2) collector layer. The WSi_x layer is deposited by CVD using a gas mixture that ensures a silicon rich as deposited layer, ($x = 2.6$), as this improves the stability of the layer during high temperature processing. As deposited the layer exhibits a sheet resistance of $56 \Omega/\text{square}$. On annealing the sheet resistance decreases significantly due to the transformation of the layer from amorphous to the more conductive tetrahedral phase of WSi_2 . The effects of annealing on the sheet resistance are summarized in Fig. 8. Initially the decrease in sheet resistance is due to the formation of a conducting polycrystalline layer. As the temperature increases, further decreases are attributed to grain growth and silicon diffusing out of the silicide layer. All anneals were carried out in a nitrogen ambient for 2 h. For a silicide layer thickness of $\sim 200 \text{ nm}$ an anneal temperature of 1000°C yields a resistivity of $50 \mu\Omega\text{cm}$, which agrees well with the $40\text{--}100 \mu\Omega\text{cm}$ range quoted in the literature. During the fabrication of the SSOI substrate the silicide layer receives the required annealing during the bond anneal to ensure a highly conductive layer.

To investigate any degradation of leakage due to the buried silicide, Fig. 9 shows reverse bias leakage ties for the collector/base junction of SSOI HBTs at different points across the wafer. The devices show some variation in the measured ties but the majority of the devices have collector/base leakage currents between 100 fA and 10 pA . For reverse biases below 2 V , these ties show a voltage dependence of approximately $V^{1/2}$, indicating that the leakage current is due to Shockley–Read–Hall

Fig. 4. Process flow for patterned groundplane SOI fabrication. The WSi_2 layer is dry etched, refilled with polysilicon, which is then planarized. A CVD oxide is deposited and polished to produce a bondable surface. This is then bonded to the polished active substrate.

Fig. 5. Cross section TEM of a completed SOI device showing the buried oxide layer, the selective Si collector and the SiGe base.

Fig. 6. Cross section TEM of the periphery of the active area for an SOI SiGe HBT.

generation in the depletion region. To extract a value of generation lifetime in the collector, a tic from the middle of the range was chosen and an iterative fitting procedure used to obtain the best fit to the measured tic. Fig. 10 shows a comparison

Fig. 7. Cross section TEM of an SSOI wafer showing the buried tungsten silicide collector layer and the polished polysilicon layer bonded to the oxidized handle wafer.

Fig. 8. Sheet resistance as a function of anneal temperature for the buried tungsten silicide collector layer. The anneal was carried out for 2 h in a nitrogen environment.

of the fitted and measured collector/base reverse I - V tics, and an excellent fit is obtained for a lifetime of 90 ns using a

Fig. 9. Measured reverse collector/base diode characteristics of devices containing a buried tungsten silicide collector layer (SSOI devices).

Fig. 10. Comparison of measured and fitted reverse collector/base diode characteristics of devices containing a buried tungsten silicide collector layer (SSOI devices).

value for collector doping of $7 \times 10^{17} \text{ cm}^{-3}$ derived from a reverse-bias capacitance–voltage measurement and corroborated by SIMS profiling. This value of generation lifetime does not indicate significant degradation due to metal induced deep-levels so it can be stated that the buried silicide layer has not had a serious impact on collector leakage. The variability in the collector current could either be due to the presence of the buried silicide, to the selective epitaxy process used for the growth of the collector or to a combination of the two. It is difficult to distinguish between these two possibilities without further work.

Fig. 11 shows a typical output characteristic of a SiGe HBT with a tungsten silicide buried collector layer (SSOI HBT), as shown in Fig. 1. For simplicity of processing, the device did not include a buried silicide groundplane. The value of collector resistance can be estimated from the slope of the characteristic at low values of collector/emitter voltage. For the characteristic shown, a value of collector resistance of 150Ω was obtained. To investigate the variation of collector resistance across the wafer, measurements of collector resistance were made at a selection of chip sites across the wafer,

Fig. 11. Typical output characteristic of a SiGe HBT fabricated over a buried tungsten silicide collector layer (SSOI device). The emitter area was $15 \times 15 \mu\text{m}$.

TABLE I
COLLECTOR RESISTANCE ON DIFFERENT CHIP SITES FOR SiGe HBTs
FABRICATED OVER A BURIED TUNGSTEN SILICIDE COLLECTOR LAYER (SSOI
DEVICES). THE EMITTER AREA WAS $15 \times 15 \mu\text{m}$

Chip site	Collector resistance, $R_c(\text{norm})$ Ω
1b	255
3b	180
5b	90
5f	128
7d	248
7h	136

and values are summarized in Table I. Extracted values of collector resistance lie within the range $90\text{--}255 \Omega$. These values are high compared with typical values for SiGe HBTs on SOI substrates, which are typically between 17 and 35Ω [16], [19]. Fig. 1 shows that number of terms contribute to the value of collector resistance, including the vertical series resistances of the n-Si collector, the wafer bonded n-Si active layer and the n+ buried layer beneath the SiGe base, the lateral resistance of the buried silicide layer, the vertical series resistances of the n+ buried layer, the wafer bonded n-Si active layer and the n+ collector contact, and finally contact resistance. Since the lateral series resistance of the buried silicide layer is very small, the dominant terms are likely to be the vertical resistances of the n-Si active layer and the n-Si SEG layer. Of these two terms, the resistance of the n-Si active layer is likely to be the cause of both the high values of collector resistance and the variability in the collector resistance across a wafer, because it is difficult to accurately control the thickness and the uniformity of the collector layer using the grind and polish processes. More reproducible values of collector resistance could be obtained by diffusing the n+ buried layer up to the surface of the active Si wafer during the bond anneal. In this case, nonuniformities in the grind and polish process would give rise to variations in the thickness of the n+ buried layer, which should be a small component of the collector resistance. The value of collector resistance would then be determined by the thickness of the selective Si collector layer, and since this layer is grown by epitaxy, variations in thickness across a wafer should be small.

V. CONCLUSION

A technology has been described for the fabrication of SiGe HBTs on wafer-bonded SOI substrates containing a buried tungsten silicide layer for collector resistance reduction or a buried silicide groundplane for crosstalk suppression. A resistivity of $50 \mu\Omega \cdot \text{cm}$ has been achieved for a buried tungsten silicide layer after an anneal of 120 min at 1000 °C. Contamination issues associated with the buried tungsten silicide layer have been investigated by characterizing the collector/base reverse I - V tics of SiGe HBTs. Leakage currents in the range 100 fA and 10 pA are measured and a generation lifetime of 90 ns is obtained by fitting a tic from the middle of the leakage current range. This value of lifetime is consistent with the collector doping concentration of $7 \times 10^{17} \text{ cm}^{-3}$, and indicates that the buried silicide layer does not have a serious impact on junction leakage current. Collector resistances have been measured on SiGe HBTs and found to vary from 90 to 255 Ω across a wafer. This variation has been attributed to nonuniformities in the grind and polish processes. A solution to this variation has been proposed in which the buried n+ layer is diffused to the surface of the silicon during the bond anneal.

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thermal CVD, GTOs, and static induction thyristors. Major activity at present is the use of direct silicon wafer bonding for producing silicon-on-insulator (SOI) substrates for low-power bipolar transistor circuits. This includes trench and refill before bond technology and buried metallic layers to eliminate epitaxial layers and to minimize collector resistance. Ground plane SOI structures incorporating tungsten silicide layers are being investigated for crosstalk suppression in mixed signal circuits and for ultrashort MOSTs. The silicon wafer bonding combined with the integrated circuit patterning techniques is also being applied to micromachining applications such as sensors, mechanical actuators and 3-D-mm wave components. Other projects include epitaxial Si and SiGe growth for deep submicrometer SOI for FDMOSTs, thin-film transistors in polysilicon or bonded silicon on glass for displays and imagers, magnetic layers and high density interconnects produced by sputtering and CVD for ICs and MR heads. He has coauthored over 250 publications in the area of silicon/device technology. In 1992, he was promoted to Professor of Microelectronic Engineering and is at present Director of the Northern Ireland Semiconductor Research Center.

B. M. Armstrong received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from Queens University, Belfast, U.K., in 1973 and 1969, respectively.

He is currently a Reader in Microelectronics at Queens University and Deputy Director of the Northern Ireland Semiconductor Research Center. He has published approximately 150 papers. His research has been in the field of silicon wafer bonding, SOI technology, high-frequency low-power bipolar devices, and MOS technology and devices. His

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Peter L. F. Hemment (M'84) received the B.Sc., Ph.D., and D.Sc. degrees from the University of Surrey, Guildford, U.K.

He is currently an Emeritus Professorial Research Fellow in the School of Electronics and Physical Sciences, University of Surrey. He has more than 30 years experience in semiconductor processing, specializing in the application of ion beams for the modification and analysis of silicon and related materials. His research initially caused him to address the engineering issues of quality control, then

during the 1980s he investigated compound synthesis by high-dose reactive ion implantation and was instrumental in the development of SOI/SIMOX technology. He is internationally recognized for his contribution to the development of SIMOX technology. Subsequently, he investigated applications of SOI materials and the control of extended defects in synthesized Si-SiGe-Si heterostructures, suitable for MOS and bipolar device applications, formed by Ge⁺ implantation into silicon. He has acted as a consultant to the silicon industry, has played an active role in the management of major EU programmes and is committed to furthering international academic collaboration.

Dr. Hemment is a Fellow of FInstP and FIEE, and a chartered member of the Institute of Physics and the Institution of Electrical Engineers.

Steven Hall (M'93) received the Ph.D. degree in integrated injection logic in the GaAs–AlGaAs materials system from the University of Liverpool, U.K., in 1987.

He then joined the lecturing staff, University of Liverpool, where he began work on SOI materials characterization and device physics, subsequently obtaining funding to work in these areas on the SIMOX and oxidized porous Si systems. The work was in collaboration with U.K. university and industrial collaborators. Other areas of activity concerned fabrication and electrical assessment of cobalt disilicide Schottky diodes together with silicon–germanium materials characterization and device physics for both bipolar transistor and MOSFET. The SiGe work currently concerns high-performance analog bipolar and new forms of low-voltage logic with particular interest in modeling and associated materials characterization. Current SOI work is in the area of low-voltage/low-power integrated circuits both SiGe HBT and MOS. His other major activity concerns novel design concepts for very deep sub-micrometer vertical MOSFETs. He is currently Head of the Department of Electrical Engineering and Electronics and serves on a number of U.K. advisory groups.

Peter Ashburn (M'98) was born in Rotherham, U.K., in 1950. He received the B.Sc. degree in electrical and electronic engineering and the Ph.D. degree in experimental and theoretical study of radiation damage in silicon p-n junctions from the University of Leeds, U.K., in 1971 and 1974, respectively.

In 1974, he joined the Technical Staff of Philips Research Laboratories and worked initially on ion implanted integrated circuit bipolar transistors, and then on electron lithography for submicrometer integrated circuits. In 1978, he joined the Academic Staff of the Department of Electronics and Computer Science, University of Southampton, U.K., as a Lecturer, and currently is the holder of a Personal Chair in microelectronics. Since taking up a post at Southampton University, he has worked on polysilicon emitter bipolar transistors, high-speed bipolar and BiCMOS technologies, gate delay expressions for bipolar circuits, and the effects of fluorine in polysilicon emitters. His current research interests include SiGe heterojunction bipolar transistors, SiGeC and its device applications and vertical MOS transistors for application in sub-100-nm CMOS technology. He has authored and coauthored 200 papers in the technical literature, given many invited papers on polysilicon emitters, SiGe HBTs and vertical MOSFETs and has authored books on the design and realization of bipolar transistors in 1988 and on silicon germanium heterojunction bipolar transistors in 2003.