Performance Improvements in Polysilicon Source-Gated Transistors

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The source-gated transistor (SGT) is a new type of transistor in which the current is controlled by a potential barrier at the source and by a gate which modulates the effective height of the source barrier. It is an ideal device architecture to be used with the low mobility materials typically applied to large area electronics, as it provides low saturation voltages and high output impedances. Furthermore, the high internal fields and low concentration of excess carriers lead to higher speed and better stability compared with FETs, particularly in disordered, low mobility semiconductors. As such, the SGT is especially well suited to thin-film analog circuits.

In this paper we will examine SGTs in polysilicon, a semiconductor with a well developed technology. Polysilicon SGTs have been made in the past [1], but for this study the drain is aligned with the gate using a bottom gate structure on glass, back exposure and ion implantation to register the n+ drain contact to the edge of the gate. Fig.1 shows a micrograph of a self-aligned structure. The source barrier is formed using Cr metal via a source window. A cross-section of the device is shown in Fig. 2. Ideally, the structure should be symmetrical, with a drain on either side of the source. As shown by the micrograph, this is not the case, with the source-drain separation (d) to the left drain (D_1) being much smaller than that to the drain on the right (D_2). However, a useful property of the SGT is that the current is independent of d , since it is controlled by the source barrier. A self-aligned structure will, of course, minimize gate-drain capacitance.

An example of output and transfer characteristics is shown in Fig. 3. The low saturation voltages and high output impedances typical of an SGT are apparent. The output characteristics remain flat out to $V_D=20V$, with no significant degradation due to carrier generation which leads to the kink effect observed in polysilicon FETs [2]. The low saturation voltage and high output impedance (Z_O) over a large V_D range are due to the fact that the transistor pinches off at both the source ($V_D=V_{SAT1}$) and drain ($V_D=V_{SAT2}$) ends of the channel. V_{SAT1} occurs when the reverse biased source barrier depletes the polysilicon under it while V_{SAT2} occurs when $V_D=V_G-V_T$, as in a regular FET (Fig. 4); in this case $V_T\approx-43V$. To maximize Z_O for V_D between V_{SAT1} and V_{SAT2} , we need optimum design of the field plate. Above V_{SAT2} it is found that Z_O depends on d , presumably because the greater this is, the further V_D is spread and the lower the field. Intrinsic gain measurements on an SGT with $d=10\mu m$ show gains in excess of 1000 and two peaks corresponding to V_{SAT1} and V_{SAT2} (Fig. 5).

One disadvantage of the SGT compared to and FET is the temperature coefficient of the drain current. Since there is a barrier at the source, the current over/through the barrier will be thermally activated. A typical example is shown in Fig. 6(a). Above $V_G=-5V$ the barrier is pulled down by the gate as expected, but the activation energy, E_A , of $\approx 0.25eV$ is a lot more than one would expect in an FET. A solution to this problem would be to make a field emission source in which at a large gate voltage the barrier would become transparent, with carriers tunneling through the barrier at the Fermi level of the metal [3]. Using the highly developed technology available for silicon it should be possible to do this using a combination of thin insulating films and precise doping. Fig. 6(b) shows the result of an attempt to reduce E_A ; at $V_G=5V$, E_A is $\approx 0.04eV$. In this case, the current changes by 30% between 30 and 100°C.

Another important parameter is the frequency response of the transistor. Calculations have shown that for a given barrier height, f_T is proportional to the average current density through the source, J_S [4]. Since the current tends to be concentrated at the edge of the source, J_S can be increased by reducing the source length (S Fig. 2). This is illustrated in Fig.7 where the current to each drain of an SGT with $S=2\mu m$ is measured separately and compared with the current achieved when both drains are connected at the same time. The currents through D_1 and D_2 are similar at $V_D<10V$ despite a large difference in d . Furthermore, connecting both drains almost doubles J_S ; since the source capacitance remains the same, f_T will also be doubled. f_T would increase further if S was reduced. For these self-aligned devices with both drains connected, the calculated f_T is $>100MHz$.

It is shown that, by using options available with silicon technology, it should be possible to make SGTs in polysilicon of high quality in terms of intrinsic gain, temperature coefficient and frequency response.

[1] J. M. Shannon, D. Dovinos, F. Balon, C. Glasse and S. D. Brotherton, *IEEE Electron Dev. Lett.*, Vol. 26, No. 10, pp 734-736, 2005; [2] A. Valletta, P. Gaucchi, L. Mariucci, G. Fortunato and S. D. Brotherton, *Appl. Phys. Lett.*, vol. 85, no. 15, pp. 3113-3115, 2004; [3] J. M. Shannon and F. Balon, *Papers from ITC'07, Solid State Electr.*, Vol. 52, pp. 449 – 454, 2008; [4] J.M. Shannon and F. Balon, *IEEE Trans. Electron Dev.*, Vol. 56, Issue 10, pp. 2354-2356, 2009.

Fig. 1. Micrograph of self-aligned polysilicon SGT. Width $W=50\mu\text{m}$, source length $S=2\mu\text{m}$, source-drain separation $d=10\mu\text{m}$.

Fig. 2. Cross-section of the self-aligned structure.

Fig. 3. Output characteristics (a) and corresponding transfer curve (b). $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d=10\mu\text{m}$.

Fig. 4. Output characteristic showing V_{SAT1} and V_{SAT2} envelopes. $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d=10\mu\text{m}$.

Fig. 5. Intrinsic gain against drain voltage showing high gains around V_{SAT2} . $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d=10\mu\text{m}$.

Fig. 7. Drain current for the left (D_1) and right (D_2) drains on the same device (a), compared with drain current when both drains are connected (b). $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d_1=4\mu\text{m}$, $d_2=16\mu\text{m}$.

Fig. 6. Activation energy of drain current for a device with (a) $7.5 \cdot 10^{13}/\text{cm}^2$ p-type doping under the source barrier and (b) $1 \cdot 10^{13}/\text{cm}^2$ n-type. $W=50\mu\text{m}$, $S=2\mu\text{m}$, $d=10\mu\text{m}$.