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Interface passivation and trap reduction via a solution-based method for near zero hysteresis nanowire FETs

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ABSTRACT. In this letter we demonstrate a solution-based method for a one-step deposition and surface passivation of the as-grown silicon nanowires. Using *N*, *N*-dimethylformamide (DMF) as a mild oxidizing agent, nanowires' surface traps density was reduced by over two orders of magnitude from $1 \times 10^{13} \text{ cm}^{-2}$ in pristine NWs to $3.7 \times 10^{10} \text{ cm}^{-2}$ in DMF treated NWs, leading to a dramatic hysteresis reduction in nanowire FETs from up to 32V to a near-zero hysteresis. The change of polyphenylsilane nanowire shell stoichiometric composition was confirmed by XPS analysis showing 35% increase in fully oxidized Si^{4+} species for DMF-treated

nanowires compared to dry NW powder. Additionally, shell oxidation effect induced by DMF resulted in more stable NW FET performance with steady transistor currents and only 1.5V hysteresis after 1000 hours air exposure.

KEYWORDS: *hysteresis, silicon nanowires, field-effect transistor, nanowire interface, DMF, XPS, HRTEM, interface trap reduction, interface passivation*

TEXT. Silicon nanowires (Si NWs) are attractive candidates for building novel electronic devices using the “bottom-up” solvent-based processing. Their unique physical and electrical properties, including single crystal lattice structure, efficient charge transport capabilities, excellent mechanical flexibility¹ attracted considerable research attention for the fabrication of chemical and biological sensors²⁻⁴, high performance FETs⁵⁻⁷ and optical devices⁷. Leiber’s group has demonstrated charge mobility of $1350\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ using boron-doped chemical vapor deposition (CVD) grown Si NWs as semiconducting material in the field-effect transistors (FETs), emphasizing the potential for high mobility devices⁵. Oriented Si NWs can be printed and solution-processed on electrode structures on flexible substrates using various deposition techniques¹, suitable for the production of electronic devices on a roll-to-roll basis for industrial applications. This highlights their compatibility with low-temperature processing steps for plastic and printed electronics device applications such as artificial e-skin⁸ and chemical sensors⁹.

To enable truly large area printed electric devices incorporating semiconducting nanowires, a scalable NW growth technology is required. CVD-based growth methods struggle to deliver significant amounts of NWs powder due to limited substrate size and the high-cost of growth processes. On the contrary, a Supercritical Fluid-Liquid-Solid (SFLS) method¹⁰ has the ability to tune the NW synthesis and to be scaled-up for kg/day production, suitable for industrial

applications ¹¹. However, the SFLS grown Si NWs are covered with an amorphous polyphenylsilane shell during the synthesis. The shell is mostly composed of carbon, oxygen and silicon species, as we discuss later, with silicon being in various oxidation states (Si^{1+} , Si^{2+} , Si^{3+} , Si^{4+}), contributing to the nanowire surface states that play important role in electronic properties, and can dramatically affect NW devices performance such as FETs. Trapping of charge carrier at semiconductor-dielectric interface, including nanowire shell region can lead to a hysteresis effect in devices I-V characteristics and low charge mobility.

Hysteresis in nanowire, carbon nanotube and organic based FETs, especially utilizing SiO_2 dielectrics, is the main source for performance instabilities that affects the reproducibility and reliability of the devices. Hysteresis represents a shift in the threshold voltage (V_{th}) under the application of gate bias.

The hysteresis behaviour mainly originates from electron and holes trapping/detrapping at the semiconductor/insulator interface due to dielectric surface functionalities and adsorbed small molecules (e.g. oxygen and water) by the silanol groups at the interfacial layer between the semiconducting material and the gate dielectric ¹². These silanol groups (Si-OH), also known as hydroxyl groups, can be formed at the silicon oxide surface even during the synthesis of silica ¹³, and not just through atmospheric exposure. High density of water molecules at SiO_2 surface was shown to induce a hysteresis exceeding 50% of the applied gate voltage in carbon nanotube FETs ¹⁴. Additionally, hole trapping can originate from weak Si-Si bonds (excess silicon or oxygen vacancies) and weak Si-O bonds (siloxanes) near the Si- SiO_2 interface ¹⁵.

In nanowire FETs hysteresis can be observed both in moisture-free (dry glove box) and ambient air conditions and is associated with strong bonding of polar water molecules to SiO_2 surfaces of nanowires and substrates.

Annealing Si NWs at 700 °C ¹⁶ and ~ 1100 °C ¹⁷ in an oxygen environment was reported to form a SiO₂ passivation layer around the nanowires, reducing the hysteresis caused by the surface states. However, such high temperature annealing is not suitable for plastic electronics applications, and a low-temperature process is still required.

In this work, the hysteresis effect in solution processed SFLS grown Si nanowire FET devices was investigated and a room-temperature solvent-based oxidising-agent treatments was applied to demonstrate reproducible bottom-gated NW FETs with very low/nearly-zero hysteresis. The choice of solvents had a dramatic impact of the nanowire surface traps, and as shown for DMF, the trap density was reduced by over two orders of magnitude.

The undoped (intrinsic) Si NWs were grown via Supercritical Fluid-Liquid-Solid (SFLS) with monophenylsilane as a reactant in supercritical organic solvents ¹⁰. The Si NWs have a single crystal Si core and an amorphous polyphenylsilane shell mainly composed of carbon (C1s) (44%), oxygen (O1s) (39%) and stoichiometric silicon (Si2p) (15%) as verified by our XPS analysis (Supporting Information (SI) Figure S2, Table S1), and consistent with previous reports ¹¹. We used a bottom-gated FET configuration where the NWs were deposited and aligned between device electrodes in a one-step process using dielectrophoretic (DEP) self-alignment of nanowires dispersed in a solvent with the application of alternating electric field ¹⁸ [see the Supporting Information (SI) for devices fabrication]. The complete device structure is shown in Figure 1. Over 20 solvents were investigated to produce dispersions of nanowires, but only DMF and DMA (dimethylacetamide) have shown pronounced nanowires oxidation/passivation effects resulting in significant improvement of NW transistor performance. For the studies presented in this paper anisole was used as a reference solvent for the nanowire dispersions.

Figure 1. (a) Schematic diagram of the FET device, showing the NWs aligned across the channel area and the double-layer Au ohmic contacts, where doped Si substrate serves as the common –gate electrode. (b) Transfer characteristic of the bottom-gated Si NW FET showed in linear and log-linear scales. The arrows show the direction of the gate voltage scan. High hysteresis of 30V (black line) was exhibited when NWs are dispersed in anisole and very low hysteresis of 0.9V when dispersed in DMF (red line), due to significant reduction of the hole traps.

NW FETs were characterised using semiconductor parameter analyser Kiethley 4200 SCS, in a dry N₂-filled glove box – to eliminate environmental effects causing degradation of the devices, and stability measurements were conducted in ambient air conditions. The change of the gate bias sweeping direction from forward to backward induced a shift in the threshold voltage, which was estimated for the extraction of the hysteresis value [see Supporting Information (SI) for nanowires hysteresis measurements].

The hysteresis values were obtained as the magnitude of threshold voltage shift during the forward ($V_{th_forward}$) and reverse ($V_{th_reverse}$) sweeps of the gate voltage (V_G) $\Delta V_{th} = V_{th_reverse} - V_{th_forward}$. The hysteresis is associated with the traps through the relation $\Delta V_{th} = \frac{\Delta Q_{trap}}{C_i}$ ¹⁹, where ΔQ_{trap} is the amount of trapped charge and C_i is the capacitance of the gate insulator.

The hysteresis values were extracted from the linear regime FET transfer characteristics. (Supporting Information (SI) Figure S1)

Figure 1 (b), demonstrates typical transfer characteristics data for Si nanowire FETs prepared using anisole and DMF as processing solvents. Anisole-processed NW FETs showed very large threshold voltage shift for forward and reverse gate voltage scans, whereas DMF processed devices demonstrated very small changes between the forward/reverse scans, and the transistor current at higher gate voltages (V_G -25 to -40V) was typically higher than the current in devices with anisole dispersed nanowires. The difference in hysteresis is significant and is attributed to the reaction of the dispersion solvent with the NW shell. Over 100 devices were fabricated and characterised during this work, and all of them showed the consistent trend where devices fabricated using DMF as a solvent exhibited a significant reduction in hysteresis compared to transistors fabricated with anisole. Based on a statistical analysis of typical 15 bottom-gated FET devices prepared with each solvent, the average hysteresis values (ΔV_{th}) of NWs dispersed in DMF and anisole were 3V and 25V respectively (Supporting Information (SI) Figure S3 (a), Table S2).

The charge trap density (Q_{trap}) and the carrier mobility (μ) were estimated using the following equations^{6, 20-22}:

$$qQ_{trap} = \frac{C_{NW}|\Delta V_{th}|}{2\pi(Nr_{nw})L} \quad (1)$$

$$C_{NW} = N \times \frac{2\pi\epsilon_o\epsilon_r L}{\cosh^{-1}(\frac{r_{nw}+d}{r_{nw}})} \quad (2)$$

$$\mu = \frac{L^2}{C_{NW}} \frac{1}{V_D} g_m \quad (3)$$

Where q is the elementary charge, C_{NW} is total gate capacitance based on the cylinder-on plate model which takes into consideration the electrostatic fringing effect^{6, 21}, ΔV_{th} is the hysteresis, N is the number of NWs crossing the FET channel, r_{nw} is the radius of the nanowire (~15nm, TEM results), L is the length of the nanowire in the FET channel (10 μ m), ϵ_o is the absolute permittivity, ϵ_r is the dielectric constant of the gate insulator (~3.9) and d is the thickness of the gate dielectric (~230nm). In the equation (3), g_m is the transconductance and V_D is the applied source-drain voltage. Equation (1) was modified, taking into consideration the total number (N) of aligned NWs across the channel.

The density of occupied traps for the devices shown in Figure 1(b) was calculated using equations (1-2). Q_{trap} value of $1.2 \times 10^{13} \text{ cm}^{-2}$ was found for the anisole-treated NW FET, with ~120 NWs in the FET channel, whereas the trap density in DMF-treated NW FET (with ~40 NWs) was $3.7 \times 10^{11} \text{ cm}^{-2}$, demonstrating significant reduction of traps following DMF passivation. The results for some of the lowest trap density, $3.7 \times 10^{10} \text{ cm}^{-2}$ achieved with DMF dispersed nanowire FETs (Figure 2 (a, b)), showed nearly-zero hysteresis of 0.1V and ohmic output characteristics. Statistical analysis of over 30 nanowire FETs fabricated with anisole and DMF solvents demonstrated relatively wide spread of hysteresis values (ΔV_{th}) between 21V and 32V corresponding to trap densities 8.6×10^{12} to $1.3 \times 10^{13} \text{ cm}^{-2}$ for anisole dispersed NWs. (Supporting Information (SI) Figure S3 (a)). On the contrary, the DMF dispersed nanowire

FETs showed significantly narrower hysteresis results between 0.1V and 5.1V corresponding to Q_{trap} values of 3.7×10^{10} to $2.1 \times 10^{12} \text{ cm}^{-2}$ (Supporting Information (SI) Figure S3 (b)).

Figure 2. I-V characteristic of DMF-treated Si NW FET with 15 nanowires in the channel. (a) Transfer characteristics obtained at $V_D = -0.5\text{V}$ showing a very low hysteresis of 0.1V and device mobility of $15 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Eq. 3). (b) The output characteristics show an ohmic linear behaviour of drain current vs drain voltage bias, and also good gate modulation. V_G is increased in -5V steps from -10V to -40V.

The hysteresis effect was also investigated for nanowire devices exposed to ambient air for prolonged periods of time. ΔV_{th} was monitored for DMF-treated FET for over 1000 hours, and the hysteresis has steadily reduced from 8V to 1.5V during this period (Supporting Information (SI) Figure S3 (c, e)), indicating good channel passivation from ambient species including water molecules. Additionally, the transistor current has marginally increased from $1.2\mu\text{A}$ to $1.6\mu\text{A}$ (Supporting Information (SI) Figure S3 (d)).

Anisole treated FET device, on the contrary, showed an increase of more than 10V hysteresis in the initial 24 hour period exposure to air. However, the device current has dropped 5 times

during this short exposure, indicating a degradation of FET characteristics (Supporting Information (SI) Figure S4).

Overall, the hysteresis behaviour in our devices was consistent with previous reports for Si NW FETs, exhibiting an anti-clockwise hysteresis when during the forward gate voltage scan the long-lived traps are populated with the majority carriers holes, and the FET threshold is then pushed to higher gate voltages, as exhibited by the reverse scan. The traps are considered to be located at the interfacial surface layer of Si nanowire channel and the bottom gate dielectric (SiO_2). The traps are mainly associated with the defects of the semiconducting nanomaterials, dielectric surface functionalities and the adsorbed water and oxygen molecules at/in the interfacial layers ¹². We speculated that DMF treatment is not likely to cause changes in the silicon core structure, and the observed reduction of hysteresis is associated with the nanowire polyphenylsilane shell composition.

For the investigation of the NWs surface passivation, high-resolution X-ray Photoelectron Spectroscopy (XPS) technique was used to analyze the surface of the as-synthesised, DMF- and anisole- treated NWs [see the Supporting Information (SI) for Nanowire characterisation]. Figure 3 (a) illustrates the peak shapes of the $\text{Si}2p$ spectra of each sample with the vertical lines showing the five different Si sub-peaks including the spin-splitting peak Si^0 (elemental Si), the sub-stoichiometric oxides Si^{1+} (Si_2O), Si^{2+} (SiO), Si^{3+} (Si_2O_3) and the silicon dioxide peak Si^{4+} (SiO_2) ²³, fitted using the Gaussian/Lorentzian function (Supporting Information (SI) Figure S5 (a-c)), where the peak positions agree with the work of Bashouti *et al.* ²⁴⁻²⁵. By overlaying the peak line shapes we have observed a substantial difference in the oxidation states of the DMF-treated Si NWs shell compared to the as-synthesised (dry) and anisole-treated Si NWs. Following DMF treatment, the main peak position of the $\text{Si}2p$ XPS high resolution scan shifts

from 100.3 eV (for dry Si) and 101.2 eV (for anisole-treated Si) to 103.2 eV, which corresponds to the formation of SiO₂ (Si⁴⁺)²³.

Figure 3. (a) XPS high resolution spectrum of the Si_{2p} region of SFLS grown Si NWs dispersed in anisole and DMF. The dashed lines indicate the different oxidation states of Si⁰, Si¹⁺, Si²⁺, Si³⁺ and Si⁴⁺. After DMF treatment, Si⁴⁺ peak increases significantly, whilst anisole treatment results in a small increase in Si peak compared to the dry sample. (b) HRTEM (HITACHI HD-2300A STEM) image of Si NWs dispersed in DMF showing single crystal silicon core with 30nm diameter and ~5-8nm thick amorphous oxidized polyphenylsilane shell.

In relation to the reference sample - dry NWs, the DMF treatment has the greatest impact on the oxidation of the NWs shell showing a 35% increase in the SiO₂ peak (Si⁴⁺), and further reduction of the other peaks, except the Si₂O₃ (Si³⁺), which stays relatively constant to the reference (Tables S3-4). Also, the decrease in the core silicon (Si⁰) peak (-8%) in the DMF-treated NWs suggests that the silica content has also increased compared with the anisole-treated NWs (Si⁰

+6%). Furthermore, the decrease in the Si^{1+} (-20%) and Si^{2+} (-5%) states, indicates that the majority of the SiO_2 (Si^{4+}) increase has come from the early oxidization stages (Si^{1+} , Si^{2+}) (Supporting Information (SI) Table S3-4).

Anisole-treated NWs, when compared to the reference, show a slight decrease in Si^{1+} and Si^{3+} , with a slight increase in the Si^{2+} and Si^{4+} sub-oxide peaks (Tables S3-4). This result suggests that the treatment of the nanowires using anisole either decreases the Si^{1+} and Si^{3+} oxides, or etches polyphenylsilane shell.

Overall, the XPS analysis indicates that DMF treatment decreases the concentration of the Si^{1+} , Si^{2+} silicon species contributing to the increase of SiO_2 (Si^{4+}) composition in the nanowire surface layer. Thus, the DMF solution acts as a mild chemical oxidizing agent for the polyphenylsilane shell ²⁶⁻²⁷.

According to the C1s XPS spectra, the residue of anisole (Supporting Information (SI) Figure S6 (b)) and DMF (Supporting Information (SI) Figure S6 (c)) can be observed due to the increase of C-C and C=C for anisole due to the presence of the aromatic ring, and the C=O in DMF.

Following the XPS analysis, Si NWs were characterised by HRTEM (HITACHI HD-2300A STEM). Figure 3(b) shows an image of a typical nanowire, with 30 nm diameter single –crystal core. The light grey colour layer around the Si core indicates the presence of a 5-8nm thick oxidised amorphous shell. The increase of silica amount (SiO_2) is likely to passivate the Si core channel area, and to provide stability against environmental ageing and to prevent the adsorption of water molecules that are responsible for the hysteretic behaviour of the nanowire FET device. However, it is expected that the non-uniformity of the shell contributes to the variations in the low-hysteresis behaviour of our devices. Additionally, the oxide shell can act as a gate dielectric

providing an improvement in the interfacial properties between Si NW core and the gate dielectric (SiO₂). Furthermore, due to the reduction of trap states after DMF treatment and the corresponding increase of the transistor current (Figure 1 (b)), the FETs on/off ratio between the current in the 'on' state and 'off' is increased.

We further investigated whether the passivation mechanism of DMF was applicable to NWs that have already been treated in anisole. Bottom-gated FETs were fabricated with NWs dispersed in anisole and then treated in DMF for a short period of time. The hysteresis reduced from 11V to 6V when the FET device was dipped into DMF for 10 seconds, in ambient air (Supporting Information (SI) Figure S7 (a)). An increase of the FET performance was also observed, with the output current (I_{OUT}) increasing from $\sim 0.95\mu A$ to $\sim 4.3\mu A$ (measured in N₂-filled glove box) (Supporting Information (SI) Figure S7 (b)), and an increase in the device mobility (μ) from $1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ to $8\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. The reduction of the hysteresis indicates the fast formation of the oxide shell when the NWs are exposed to DMF, providing stability to the FET performance. Then, the device was exposed to ambient conditions for 1000 hours and the hysteresis only marginally increased by 0.6V with a further increase in the device mobility to $9\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and in the output current (I_{OUT}) to $\sim 5.8\mu A$ (Supporting Information (SI) Figure S7 (c, d)) highlighting the passivation effect of DMF on the polyphenylsilane nanowire shell. A shift of the threshold voltage to the positive was also observed (Supporting Information (SI) Figure S7 (c)) after the stability test in ambient air, from $V_{th} = -9V$ to $-6V$, verifying the passivation of the NWs interface and reduction/elimination of the number of occupied traps, which cause the screening of the gate electric field. Based on a statistical analysis of 10 samples, an increase in the device mobility (μ) was also observed (Supporting Information (SI) Figure S8). Dimethylacetamide (DMA) and *N*-Methylformamide (NMF) treated Si NWs were also investigated, with DMA

achieving similar results to DMF, but their surface analysis needs further investigation. Also, DMF-treated CVD grown Si NWs showed similar results with DMF-treated SFLS grown Si NWs, with less than 2V hysteresis in N₂ environment and less than 1V when exposed to ambient conditions, further demonstrating passivation effects of DMF for different types of nanowires.

As a final step, we have fabricated bottom gate Si nanowire FET devices on plastic substrates (Kapton) to investigate compatibility of DMF passivation for plastic electronic devices. The NW FETs with parylene N gate insulator and DMF processed nanowires demonstrated similar hysteresis values (~2.5V) Supporting Information (SI) Figure S9) to the transistors with SiO₂ dielectric. DMF did not seem to affect the organic gate dielectric or the substrate.

In summary, we have experimentally demonstrated the effect of DMF solution acting as mild oxidizing agent and passivation for Si nanowire shells resulting in a drastically suppressed nanowire FET hysteresis. This chemical method can be conducted at room temperature, compatible with the fabrication of nanowire electronic devices on various substrates including plastics. Bottom-gated FET devices fabricated with silicon NWs dispersed in DMF exhibited low hysteresis, on average, ~8 times lower as opposed to using anisole as a dispersant. The hysteresis reduction of over 300 times (from 32V to 0.1V) was demonstrated with near zero hysteresis devices obtained with DMF treated MPS Si NWs.

DMF-treated NWs exhibited a one-to-two orders of magnitude trap-density decrease compared to anisole-treated NWs and an increase in device mobility. DMF-treated devices showed environmental stability, with a further decrease of the hysteresis even after 1000 hours of exposure as opposed to the anisole-treated devices. However, a sharp increase in hysteresis was observed for anisole-processed NW FETs after exposure to air.

Based on the XPS data, a significant 35% increase of SiO₂ composition of nanowire shell around the core is demonstrated after DMF treatment, passivating the Si core. The dramatic reduction of hysteresis following the DMF processing indicates that the modified nanowire shell prevents the adsorption of water molecules on the surface of the Si core, which is the main source of hysteresis. The shell-passivation of Si NWs with DMF considerably improves the fabrication of reliable and reproducible Si NW devices demonstrated with field-effect transistors, suitable for printed nanomaterials electronic applications. The nanowire passivation approach can be extended to other nanowire applications including supercapacitors, photovoltaics and photodiodes.

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ASSOCIATED CONTENT

Supporting Information. Experimental section for NW FET device fabrication, XPS sample preparation, NW hysteresis measurements and NWs characterization. FET electrical and trap

density characterization, XPS spectra analysis, NW devices mobility statistical analysis. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Supporting Information

Interface passivation and trap reduction via a solution-based method for near zero hysteresis nanowire FETs

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Experimental Section

Hydrous *N, N*-Dimethylformamide (319937) and anisole (123226) were purchased from Sigma-Aldrich Chemicals and used for dispersing the nanowires as received.

Device's fabrication: Bottom-gated FETs were fabricated following the “bottom-up” approach. The n^{++} -doped Si/SiO₂ substrates, with thermally-grown SiO₂ gate dielectric, 230 nm thick, were solvent cleaned by sonication in acetone, IPA and methanol for 10 minutes each and O₂ plasma cleaned (100W) for 5 minutes. The patterning of the source/drain bottom-electrode contacts was performed via photolithography (lift-off). Gold (Au) micro-electrodes, were prepared by first sputtering 2nm titanium (Ti) adhesion layer followed by 50nm gold on the substrate (JLS MPS 500 Loadlocked Sputter Coating). NWs dispersions were prepared with anisole and *N, N*-dimethylformamide (DMF). The NW were aligned via dielectrophoresis (DEP), by applying an AC field ($10V_{\text{peak-peak}}$) across the two parallel source and drain electrodes with 10 μm gap. A NW “ink” drop was deposited using a syringe and nanowires were aligned across the source/drain electrodes. After the NW deposition, Au top-contacts (80nm thick) with same channel gap were deposited on the NWs, using a second photolithography (lift-off) stage. Then, the devices were annealed at 250°C for 1 hour in a N₂-filled glove box, to improve the integrity of the electrode contacts over the NWs and to evaporate residual water/solvents trapped on their surfaces. During the I-V FET measurements highly doped Si substrate served as the gate electrode.

For the XPS measurements, Si/SiO₂ substrates were cut into pieces and cleaned using solvents and O₂ plasma ash method as described previously. 50nm thick palladium (Pd) was sputtered (JLS MPS 500 Loadlocked Sputter Coating) on top of the SiO₂ to remove the substrate background signal. Silicon nanowires samples were prepared by drop-casting NW in anisole and DMF dispersions onto the substrates. ‘Dry’ NW samples were prepared by transferring NW powder with a spatula straight onto the substrates. XPS analysis was repeated three times on different samples of Si nanowires to confirm the reproducibility of results.

Nanowire hysteresis measurements: Electrical measurements were performed with a Keithley 4200 Semiconductor Characterisation System (SCS). The FETs transfer characteristics were measured in the linear regime with the gate voltage (V_G) swept from +10V to -40V (forward

scan) and immediately back to +10V (reverse scan) in 500mV steps. This type of V_G scan corresponds to a p-type FET being driven from the ‘off’ state to ‘on’ state and back. The value of hysteresis was extracted from the voltage difference between the reverse voltage sweep threshold voltage $V_{th_reverse}$ and the forward voltage sweep threshold voltage $V_{th_forward}$ as shown in Figure S1. Transistor measurements were performed in a dry N_2 -filled glove box and in ambient air environment at reactive humidity level of about 46%, as described in the main manuscript.

Nanowire characterisation: XPS analysis was performed using ThermoFisher Scientific (East Grinstead, UK) Theta Probe spectrometer. XPS spectra were acquired using a monochromated Al $K\alpha$ X-ray source ($h\nu = 1486.6$ eV). An X-ray spot of $\sim 400\mu m$ radius was employed. Survey spectra were acquired using pass energy of 300eV. High resolution, core level spectra were acquired using a pass energy of 50eV except for the high resolution core level spectra of Na1s where a pass energy of 100eV was employed. All spectra were charge referenced against the C1s peak at 285eV to correct for charging effects during acquisition. The manufacturer’s software (Avantage) was used to calculate the atomic percentages for the surface chemical composition. This software incorporates the appropriate sensitivity factors and corrects for the electron energy analyser transmission function. Peak fitting Si2p chemical shifts from the core Si peak were employed, where ($Si1/2 \sim \delta 0.6$) ($Si1+ \sim \delta 0.85$) ($Si2+ \sim \delta 1.7$) ($Si3+ \sim \delta 2.7$) ($Si4+ \sim \delta 3.8$), or in terms of binding energy were 99.6eV, 99.9eV, 100.7eV 101.4eV 102.5eV and 103.9eV. All ± 0.2 eV for the resolution of the data and the fit. All of the peaks were fitted using Gaussian-Lorentzian (30:70) line-shape, and the background was subtracted using the Shirley method. XPS Peak 4.1 was the software used for the fitting.

The TEM microscopy of the nanowires was performed using a HRTEM microscope (HITACHI HD-2300A STEM). The samples were prepared by drop casting the Si NWs from anisole and DMF dispersions on a holey-carbon grids (Agar Scientific).

Figure S1. The linear regime transfer characteristic of a Si NW bottom-gated FET device. The difference between the reverse and forward voltage sweep threshold voltages quantifies the magnitude of hysteresis $\Delta V_{th} = |V_{th_reverse} - V_{th_forward}|$.

Figure S2. XPS Survey spectrum of SFLS grown Si NWs on a palladium (Pd) coated Si/SiO₂ substrate, showing all elements present (C1s, Ca2p, N1s, O1s, Pd3d, Si2p) at the surface of the Si NWs.

Table S1. XPS concentration contents of the SFLS grown Si NWs.

Name	Start BE	Peak BE	Height CPS	Area (N)	At. %
C1s	289.8	285.0	281.6	214.6	43.7
Ca2p	355	348.7	346.2	3.2	0.6
N1s	405.4	404.1	397.2	7.9	1.6
O1s	537.9	532.9	529.1	192	39
Pd3d	346.4	339.4	336.8	0.7	0.1
Si2p	107.5	103.3	96.6	71.9	15

Figure S3. (a-b) Statistical analysis of the degree of hysteresis and trap density of bottom-gated FET devices with Si NWs dispersed in DMF and anisole. 15 different devices data for each solvent is presented. The DMF-treated NWs exhibited significant hysteresis reduction compared to anisole-treated nanowire devices. (c-d) Transfer and output characteristic of the DMF-treated FET device measured in N₂-filled glove box and in ambient air environmental conditions after 1000 hours of exposure. (e) Change of the hysteresis for DMF-treated FET as measured in air. Reference measurement is conducted in a dry N₂-filled glove box.

Table S2. Hysteresis (ΔV_{th}) and trap density (Q_{trap}), for Si NWs dispersed in anisole and DMF.

Device Number (anisole)	Hysteresis in Anisole (ΔV_{th})	Q_{trap} in Anisole (cm^{-2})	Device Number (DMF)	Hysteresis in DMF (ΔV_{th})	Q_{trap} in DMF (cm^{-2})
1	32	1.3E+13	1	5	2.1E+12
2	30	1.2E+13	2	4	2.1E+12
3	29	1.2E+13	3	5	1.9E+12
4	27	1.1E+13	4	4	1.8E+12
5	27	1.1E+13	5	4	1.7E+12
6	26	1.1E+13	6	4	1.7E+12
7	25	1.0E+13	7	4	1.5E+12
8	25	1.0E+13	8	3	1.2E+12
9	25	1.0E+13	9	3	1.1E+12
10	25	1.0E+13	10	3	1.1E+12
11	23	9.5E+12	11	2	1.0E+12
12	22	9.2E+12	12	2	9.8E+11
13	22	9.2E+12	13	2	7.0E+11
14	22	8.7E+12	14	1	3.7E+11
15	21	8.6E+12	15	0.1	3.7E+10

Figure S4. (a) Transfer characteristic of the FET devices with NWs dispersed in anisole and measured in N₂-filled glove box and ambient air environmental conditions after 24 hours of exposure.

The hysteresis increased from 18 V to 33 V. The measurement is conducted in air 24 hours after FET removal from the glove box. The device was unmeasurable after one week of ambient air exposure, showing no detectable FET characteristics.

Figure S5. XPS spectra of the Si2p region for (a) dry Si NW, (b) anisole-treated Si NW and (c) DMF-treated Si NW. The line shape of each sample (black) was fitted by the peak deconvolution with Si⁰, Si¹⁺, Si²⁺, Si³⁺, Si⁴⁺ components, fitted using the Gaussian/Lorentzian function. The black curves show the experimental data and the red curves show the data fits.

Table S3. XPS peak areas for dry Si NWs and Si NWs dispersed in anisole and DMF.

Silicon NW Treatment	Overall XPS Peak Areas	Si ⁰	Si ¹⁺	Si ²⁺	Si ³⁺	Si ⁴⁺
Dry	19500	6200	3900	2400	6300	700
Anisole-treated	17300	6600	2900	2500	4000	1300
DMF-treated	20400	4800	0	1500	6200	7900

Table S4. XPS percentage atomic concentrations of dry Si NWs and Si NWs dispersed in anisole and DMF.

Silicon NW Treatment	Si ⁰	Si ¹⁺	Si ²⁺	Si ³⁺	Si ⁴⁺
Dry	32%	20%	12%	32%	4%
Anisole-treated	38%	17%	14%	23%	8%
DMF-treated	24%	0%	7%	30%	39%

(a)

(b)

Figure S6. XPS spectra of the C region for (a) dry Si NW, (b) anisole-treated Si NW and (c) DMF-treated Si NW. The line shape of each sample was fitted by the peak deconvolution with C-O, C=O, C-C, C-N/C-O and Si-C/C=C components, fitted using the Gaussian/Lorentzian. (d) XPS survey spectrum of the C region of Si NWs.

According to the C1s XPS spectra, the residue of anisole (b) and DMF (c) can be observed. The increase of C-C and C=C peaks in (b) is associated with the presence of the anisole benzene ring, and the C=O peak in (c) is associated with DMF. The black curve shows the experimental data and the red curve shows the data fits.

Figure S7. (a) Transfer and (b) output characteristics of bottom-gated FETs with SFLS grown Si NWs. Devices were prepared using anisole, and then treated with DMF. Black curves correspond to FETs fabricated using *only* anisole solvent. Red curves correspond to the *same* devices that were later functionalized in DMF for 10 seconds and re-measured. As transistor devices are identical, and the measurements correspond to different solvent treatments, the effect of the number of nanowires in the transistor channel on the FET performance can be completely ruled out.

The hysteresis decreased from 11V to 6V following DMF treatment. The increase of the on/off ratio ($I_{ON/OFF}$) and the output current (I_{OUT}) (from $\sim 0.95\mu\text{A}$ to $\sim 4.3\mu\text{A}$) after DMF treatment underlines the effect of the DMF solvent on the nanowire shell interface providing lower trap density. Also an increase in the device mobility (μ) was observed from $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $8\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ after DMF treatment. (The device was measured in a N_2 -filled glove box).

(c) Transfer and (d) output characteristic of the same device after 1000 hours of exposure to ambient air environment. The hysteresis was only increased by 0.6V with a further increase in the output current (I_{OUT}) to $\sim 5.8\mu\text{A}$ and the devices mobility to $9\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

Figure S8. Statistical analysis of the increase of the device mobility (μ) of bottom-gated FET devices with Si NWs dispersed in anisole and then treated in DMF. The increase in the device's mobility (μ) is attributed to the NWs shell passivation via DMF mild oxidation. The device No 10 data is shown in Figure S7.

Figure S9. Transfer characteristic of the DMF-treated FET device fabricated on plastic substrate (Kapton) with parylene N as a gate dielectric (measured in N_2 -filled glove box). The device demonstrated hysteresis of ~ 2.5 V.